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DEVELOPMENT OF DIGITAL AND ANALOGUE SYSTEMS OF DECODING PULSE WIDTH MODULATED DATA

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SUMMARY

A flight data decoder has been developed which, in conjunction with some commercial equipment, demodulates the data signal which is separated, on playback, from a composite speech plus flight data recording taken with the A.R.L. Flight Memory Airborne Equipment. In the recording of the flight data, sampled data signals modulate the width of pulses which in turn gate a sinusoidal oscillator. Automatic presentation of the decoded flight data information, in either digital or analogue format, is possible using the decoder.

CONTENTS

1. INTRODUCTION

The A.R.L. (Aeronautical Research Laboratories) Flight Memory Equipment has been developed because of the need for a device to assist in aircraft accident investigation. Essentially, the equipment can be divided into two units, namely, the Airborne Equipment and the Ground Station Equipment. In the Airborne Equipment crew conversation and various flight parameters such as airspeed, altitude, aircraft heading and the like are multiplexed, after suitable modulation, to form a composite signal which is recorded on a single channel magnetic wire recorder. In the Ground Station Equipment, crew conversation and the various flight data parameters are separated individually. A detailed description of the Ground Station Equipment excepting the flight data decoder portion (which forms the substance of this paper) is given by Fraser.[1]

Although the flight data decoder portion may be considered as a separate entity, it is an integral part of the A.R.L. Flight Memory Ground Station Equipment which is housed within a single unit. Each module within the Ground Station Equipment has been assigned a chassis number (from 1 to 9 since there are 9 modules). Chassis numbers 5 to 9 relate to circuits which will be described in this paper. In addition, reference will be made to components on chassis number 1, which encompasses the front panel and interwiring.

2. NATURE OF TIME MULTIPLEXED FLIGHT DATA SIGNAL TO BE DECODED

The flight data signal, as recorded, consists of a series of sinewave bursts, the duration of which is modulated in accordance with the level of the parameter being sampled. The frequency of the sinewave is 3500 hertz, which is high enough to allow frequency multiplexing of the speech and data signals for single track recording, and at the same time, low enough to make possible recording on the wire recorder which restricts the high frequency performance at the wire speed chosen. A total of 8 "data" channels is used, of which 6 are used for flight data recording and the other 2 to provide calibration and synchronising information to enable the record to be decoded. At the 24 per second sampling rate used, each channel is sampled 3 times per second.

The duration of the sinewave burst is made a finite value; actually 10 cycles of the 3500 hertz signal, for a zero signal input. Negative values of input signal do not arise and hence zero signal represents the lowest possible value of signal on any channel. Maximum (100%) signal on a signal channel produces a duration of 110 cycles. Hence each cycle of the 3500 hertz signal represents 1% of the flight data transducer range. To enable synchronisation of the record on playback, one channel, known as the "marker" channel, is fed with a fixed signal which produces a duration of 120 cycles. This duration is greater than the maximum which can occur on any signal channel. Calibration is made possible using the marker channel and an additional channel, called the "zero" channel, which is fed at all times with zero signal. Channel identification numbers are as follows:

Channels 1 to 6	Signal Channels
Channel 7	Zero Channel
Channel 8	Marker Channel

A typical envelope pattern of the time multiplexed recorded data signal is presented in Fig. 1. In the passage of a pulse, such as shown in Fig. 2(a), through the data filter the sharp leading and trailing edges of these envelopes become rounded[1, 2] as revealed in Fig. 2(b). Overshoot at the leading edge and "ringing on" at the trailing edge of the filtered pulse are in evidence. The input to the decoder consists of a chain of pulses, like that of Fig. 2(b), of varying duration. The time interval between the leading edges of these pulses is a constant 1/24th second.

3. GENERAL DESCRIPTION OF VARIOUS SYSTEMS OF DATA DECODING

In the simplest method of flight data decoding, the filtered data signal (made up of a chain of sinewave bursts) is amplified and recorded directly on a high speed visicorder. By manually counting the number of cycles in each burst, and using the transducer characteristic curve, the

value of each of the sampled flight parameters may be established. In order to resolve individual cycles of the 3500 hertz signal, a very high chart speed is required (typically about 2 metres per second which provides a displacement of about 0·6 mm. per cycle of the 3500 hertz signal). Obviously this system, apart from requiring an enormous quantity of ultra-violet recording paper (which in turn requires fixing if the record is to be kept for long periods), is tedious in the extreme with respect to the counting of individual cycles of the 3500 hertz signal. For this reason, a system of automatically presenting the demodulated flight data information is essential.

Systems of automatic flight data presentation in both digital and analogue format have been developed at A.R.L. The block schema of Fig. 3 shows the various systems of data presentation. System 1 is the direct recording method alluded to in the previous paragraph, system 2 is the digital system which enables the data to be presented one channel at a time on an electronic counter and associated printer, and system 3 is the analogue system which enables all channels to be presented simultaneously on a multitrack chart recorder. The portion of the block schema of Fig. 3 within the dotted lines refers to the decoder as built at A.R.L., whereas the blocks outside this dotted line refer to commercial instruments used in conjunction with the A.R.L. decoder. A detailed description of the various systems will follow.

4. DIRECT RECORDING OF MODULATED DATA USING VISICORDER

Although extremely tedious from the point of view of extracting information, the direct recording system (system 1) offers maximum accuracy. Signal dropouts, inherent in a magnetic wire recording system of relatively low cost, can be readily observed and accounted for on a high speed recording of this type, but present considerable difficulty in the automatic systems. In view of the large amount of paper required and the tediousness of the decoding, such a system could only be justified for a small portion of the flight recording of great interest, such as the region of the recording relating to an actual air disaster.

The finite build-up and decay times of the modulated data signal (as referred to in section 2 of this paper) are produced during the passage of the modulated data signal through the data filter. However, these times are constant for each sample of the modulated data and can therefore be readily accounted for. Individual channels can be easily identified by counting from the marker channel which is readily identifiable because it has a pulse which is of longer duration than the pulse for any other channel.

5. DIGITAL PRESENTATION OF DATA

Most commercial electronic counters allow the introduction of an external frequency standard in place of the internal one. For time interval measurements, the number of cycles of the frequency standard which occur during the interval to be measured, as set by an external gating pulse (or individual trigger pulses separated in time), are counted and registered on the counter. If the input to the data decoder is fed to the "external frequency standard" terminals of an electronic counter, and a gate signal formed about a particular channel is fed to the "time interval trigger" input, then the counter will count the number of cycles which occur in each consecutive data sample from this channel. For automatic recording of consecutive readings on the particular channel selected, a digital printer may be coupled to the counter. The number of cycles in the data sample may be simply related to the value of the sampled flight parameter. Generally speaking the method described here has been used in the automatic digital decoding system.

To enable the decoder to resolve half cycles of the 3500 hertz signal, a frequency doubler (in this case a full wave rectifier) circuit has been incorporated. To ensure that the count registered by the counter is independent of counter sensitivity adjustment a Schmitt trigger circuit, which can be set to trigger at any desired level of the modulated data input signal, transforms the incoming data signal into a discrete set of constant amplitude pulses. The output of the Schmitt trigger circuit is taken to the external frequency standard terminals of an electronic counter.

The means of generation of an appropriate gate signal for the counter can be studied with reference to the block schema of Fig. 3. By suitably smoothing and clipping the output from

the Schmitt trigger in a gate forming circuit, a typical rectangular pulse width modulated waveform results. The leading edges of the waveforms so produced synchronise a multivibrator oscillator which free runs at a frequency slightly less than the incoming 24 hertz signal. Symmetrical triggering of a divide by 8 binary chain is then accomplished by the output signal from the synchronised oscillator. Simultaneously the output from the gate forming circuit is fed to a ramp generator which effectively produces pulse height proportional to the width of the incoming pulse. By taking the ramp generator output to a voltage comparator circuit set to trigger only for the marker pulse a suitable signal for synchronising the binary counter is made available. An "AND" circuit connected to the appropriate outputs of each binary via a selector switch generates a gate signal which may be used for selecting a particular channel.

5.1. Frequency Doubler

The input block (see Fig. 3) for the decoder is, for convenience, referred to as the "frequency doubler." Such a name implies a rather simple circuit as, for instance, a full wave rectifier. While it is true that a full wave rectifier is used as the basic frequency doubler (changing the 3500 hertz signal into a 7000 hertz signal) the combined input circuit is considerably more complex. Although it is used for other purposes, the frequency doubled output is generated mainly because it enables half cycle resolution of the modulated data signal to be realized.

The block schema of Fig. 4 reveals, in general form, the composition of the frequency doubler. Essentially the input data signal (or output from the data filter) is first amplified, then passed through a full wave rectifier which doubles the frequency. To provide a suitable signal for the counter "external frequency standard" terminals and also for the gate forming circuit a Schmitt trigger circuit is used. The input to the Schmitt trigger circuit follows the amplitude pattern depicted in Fig. 2(b). Evidently the number of pulses formed by the Schmitt circuit will depend on the trigger level chosen, becoming greater as the triggering level is reduced. As the leading edge of the first pulse from the Schmitt circuit also defines the leading edge of the gate signal fed to the counter, it is essential that for consistent counting the Schmitt circuit triggers at the same relative level on each sample of the modulated flight data.

Amplitude variations inherent in the record/replay systems lead to some ambiguity in the count registered by the counter. If the trigger level is set to, say, 40% of nominal amplitude, then a $\pm 10\%$ amplitude variation, occurring just when the Schmitt circuit is about to trigger, will cause a ± 1 count variation (actually $0{\cdot}5\%$ since half cycles are being counted). It is to be noted that the data filter has been designed such that 5 complete cycles (10 half cycles) lapse before the modulated data input signal builds up to full amplitude. Similar count uncertainties result by virtue of amplitude variations occurring on the trailing edge of the modulated data pulse.

Amplitude variations inherent in the input signal can be divided broadly into two types: relatively rapid fluctuations and relatively slow variations.

In the "rapid fluctuation" group there is a $\pm 10\%$ amplitude jitter produced partly by short term variations in recorder overall gain (which may be caused by roll of the magnetic recording wire, fluctuations in contact pressure between the wire and the head on either record or playback or the presence of dust particles on the head or the wire) and, partly because of the presence of a random noise signal falling within the band of the data filter. Also included in the rapid fluctuations of amplitude are signal drop-outs, arbitrarily defined here as amplitude reductions greater than 50% of normal amplitude. Measurements made with a continuous 3500 hertz note revealed that, using a Minfon P55 as a replay device, about 1 drop-out every $3{\cdot}3$ seconds could be expected. Complete signal drop-outs having a duration of up to 30 cycles of the 3500 hertz signal occur occasionally. Signal dropouts are produced if the wire separates from the head momentarily, either during record or playback. Apart from designing the decoder to minimise the tendency of the system to temporarily lose synchronism when drop-outs occur, nothing else was done regarding rapid amplitude variations.

The effect of a slowly varying type of amplitude change can be more readily eliminated. Long term variations in amplitude may be caused by any long term drift in the overall gain from record to playback. For instance, as the rotational speed of the wire spool and not the linear speed of the wire itself is governed, the signal amplitude will vary as a spool is unreeled. To eliminate the effect on the count of a long term amplitude variation an automatic gain control circuit, as depicted in Fig. 4, has been incorporated in such a way as to maintain a constant peak output from the basic frequency doubler circuit.

The operation of the complete frequency doubler circuit may be studied with reference to the circuit of Fig. 5. For details of the system of component numbering, refer to the Appendix. At various circuit points marked with a circle containing an identification number the waveforms have been drawn in Fig. 6 and will be referred to in the text. Regulated supply rails of +24 volt and −24 volt are employed. Circuit details and performance figures on these supplies are given by Fraser.[1]

Transistor Q502 and associated circuits constitute a gain controlled common emitter amplifier. As the base of Q502 is virtually fed from a voltage signal source, the stage gain will vary inversely as the input impedance of this transistor. Now the intrinsic emitter resistance r_E varies as the D.C. emitter current I_E according to the relation:

$$r_E = \frac{K}{I_E}$$

$$K = \frac{kT}{q}$$

where k = Boltzmann constant ($1{\cdot}38 \times 10^{-23}$ joule/°K)

T = Absolute temperature (°K)

q = Electron charge ($1{\cdot}60 \times 10^{-19}$ coul.)

Hence $$r_E \text{ (ohm)} = \frac{25}{I_E \text{ (mA)}} \quad \text{at } 27°\text{C.}$$

Referring to Fig. 7(b) which is a small signal equivalent circuit for the gain controlled amplifier of Fig. 7(a) we may write,

$$\text{VOLTAGE GAIN} = Av = \left|\frac{e_0}{e_1}\right| \simeq \frac{|Z_L|}{r_E} = \frac{|Z_L|}{25} I_E \quad \text{(at } 27° \text{ C)}$$

Note that Z_L is the effective impedance seen at the collector of Q502. It is the combined load made up of load resistor R510, the output impedance of Q502, and the effective input impedance of the following stage (essentially capacitive at 3500 hertz). Typically $|Z_L|$ is approximately $8K$.

Now I_E is controlled by A.G.C. control voltage V_2 according to the relation (refer to Fig. 6(a)):

$$I_E = \frac{R_1 V_2 - R_2 V_1}{R_E(R_1 + R_2)}$$

In the derivation of this expression the emitter base voltage drop of Q502 has been neglected and it has been assumed that the base current is negligible compared with the current in the divider chain.

Substituting $R_1 = 180K$, $R_2 = 120K$, $R_E = 2{\cdot}2K$ and $V_1 = 24V$, we obtain:

$$I_E = 0{\cdot}27 V_2 - 4{\cdot}37 \quad \text{mA}$$

$$\frac{\partial I_E}{\partial V_2} = 0{\cdot}27 \quad \text{mA/volt}$$

The stage has been designed for a nominal emitter current of approximately 0·5 mA for normal input level. For this value of I_E the required value of V_2 is approximately 18 volt.

Fractional change in gain per volt change in A.G.C. control voltage

$$= \frac{1}{Av}\frac{\partial Av}{\partial V_2}$$

$$= \frac{25}{I_E|Z_L|}\left(\frac{\partial Av}{\partial I_E}\right)\left(\frac{\partial I_E}{\partial V_2}\right)$$

$$= \frac{1}{I_E}\frac{\partial I_E}{\partial V_2}$$

$$= 0{\cdot}54$$

Hence a 1-volt increase in A.G.C. control voltage will approximately halve the gain of the first amplifying stage.

Additional amplification is performed via Q503, whilst L601 and associated diodes constitute a full wave rectifier. Q601 acts simply as an emitter follower. The negative going rectified

waveform appearing on the emitter of Q601 is drawn in Fig. 6, waveform No. 2; it has an envelope pattern identical to the input signal amplitude pattern which can be observed in Fig. 6, waveform No. 1.

Peak amplitude sampling of the output of Q601 is performed via diode D501 and associated filter circuit. The filter has a charge time constant of approximately 0·5 second and a discharge time constant of approximately 1 second. Hence a D.C. voltage will be formed at the base of Q506 which follows the peaks of the rectified data signal. Transient peaks are ignored by the filter because of the relatively long charging time.

Emitter follower Q506 acts as an impedance buffer for the amplitude sampling side of the D.C. differential amplifier formed by Q504, Q505 and associated circuit. Potentiometer R102 (Gain 2 adjustment) sets up a reference D.C. voltage, typically about $-5V$ on the other side of the differential amplifier. If a difference voltage exists between the signal amplitude sampling side and the reference side of the differential amplifier a change in output voltage will appear on the collector of Q505. This voltage is the A.G.C. control voltage and is phased such that the gain of Q502 will be changed so as to make the output amplitude very nearly equal to the reference level set by R102. With this feedback gain controlled system a 300% change in input level results in a $7\frac{1}{2}\%$ change in rectified output level.

Switch S107 enables the equipment to be operated with the A.G.C. control "on" or "off." As the A.G.C. circuit takes some seconds to stabilise, it is sometimes inconvenient to operate in this mode when an immediate response is required. Normally R103 (Gain 1 adjustment) is adjusted, with the A.G.C. in the "off" position, to give the appropriate output level. If the A.G.C. circuit is then switched in, the amplitude level will be maintained in spite of any drifts which may occur in the input amplitude.

The amplitude stabilised signal appearing on the emitter of Q601 is taken to the Schmitt trigger circuit made up of Q602, Q603 and associated components.Potentiometer R604 enables the triggering level to be varied. Typically a triggering level of 2 volts (40% of input amplitude) is used as illustrated in Fig. 6, waveform No. 3. A chain of square pulses appears at the output of the Schmitt trigger circuit as illustrated in Fig. 6, waveform No. 4. The output of the Schmitt trigger circuit is capacitively coupled via C602 to the Counter External Frequency terminals.

5.2. Gate Forming Circuit

Basically the function of the gate forming circuit is to produce square pulses which follow the envelope pattern of the batches of pulses appearing at the output of the Schmitt trigger circuit. Pulses from the Schmitt circuit pass through diode D603 (see Fig. 8) and charge capacitor C603. Since the output pulses from the Schmitt circuit are effectively "off" pulses, the charging time constant of C603 will be the product of the Schmitt load resistor R607 (10K) and charging capacitor C603 (1K). Hence the charging time constant will be 10 microsecond (compare with pulse repetition period of 143 microsecond). It follows, therefore, that the charging time is negligible compared with the Schmitt pulse repetition period.

In Fig. 9, waveform No. 5, the effect of filtering the output of the Schmitt trigger circuit can be observed. Normally (no pulse input) Q604 is held off by reverse bias via R609. When the voltage across C603 reaches approximately -11V, the base of Q604 will become forward biased and this transistor will be switched on. Negative pulses arriving via D603 will charge C603 to approximately the negative supply voltage (-24 volt). When the Schmitt circuit output reverts to the "on" state between pulses, D603 will become reverse biased and C603 will discharge towards zero volts with time constant of approximately 150 microsecond {C603(1K) multiplied by R608(150K)}. Typically C603 may discharge to about -17 volt before the next pulse arrives (see waveform No. 5 in Fig. 9). Note that this voltage will depend on the triggering level set by the Schmitt trigger circuit, becoming higher in magnitude as the trigger level is reduced.

Subsequent to the arrival of the final pulse, C603 will discharge towards zero volts with time constant 150 microsecond until the switching level of -11 volt for Q604 is reached. At this voltage, Q604 will switch off and the impedance as seen at the base will be high. From this point C603 will charge towards $+24$ volt with a time constant of approximately 540 microsecond {(R608 + R609) × C603}. When approximately -2 volts across C603 is reached, however, the voltage will become clamped to the voltage output from the Schmitt trigger circuit via diode D603.

Waveform 6 of Fig. 9 illustrates the square pulse appearing at the output of the gate forming circuit. The leading edge of this waveform is virtually coincident with the leading edge of the

first pulse from the Schmitt circuit whereas the trailing edge of this waveform lags the trailing edge of the final pulse from the Schmitt circuit by approximately 120 microsecond, which is slightly less than a half cycle period of the 3500 hertz signal. Because of loading due to the ramp generator circuit the "off" level is −13 volt approximately.

5.3. Ramp Generator

Basically, the function of the ramp generator circuit is to convert the pulse width modulated signal from the gate forming circuit into a form of proportional pulse height signal. For the digital system, the signal produced by the ramp generator is used in conjunction with a voltage comparator circuit to provide a synchronising pulse each time the marker pulse arrives. As such, the demand on linearity (in respect of the relationship between pulse height and pulse width) is not very stringent for the digital system. However, for the analogue system any non-linearity in the ramp produces a non-linearity in the analogue signal. Hence linearity of the ramp is of prime importance.

The complete circuit of the ramp generator is drawn in Fig. 10. If capacitors C702 and C703 are replaced by a single capacitor, and resistor R705 plus diodes D702 and D703 are removed, a bootstrap sweep circuit similar to the one described by Williams[3] takes form.

A simplified circuit of the ramp generator is drawn in Fig. 11(a). Transistor Q701 acts merely as a switch gated by the output from the gate forming circuit. For simplicity, the transistor switch in Fig. 11(a) has been replaced by an ideal switch S. In the periods between pulses, the output of the gate forming circuit is sufficiently negative to ensure that Q701 is on (switch S closed). When Q701 is on, capacitor C701 charges via diode D701 to practically the full supply voltage. When a pulse appears at the output of the gate forming circuit Q701 switches off and capacitor C701 begins to discharge via resistor R, capacitor C, the −24 volt supply, the collector load resistor of Q702, and finally transistor Q702. Since the emitter base voltage of Q702 remains practically constant as C charges, and if it is assumed that the capacitance of C701 is so high that the voltage charge across it is negligible during the period for which S is off, a constant current of about V/R will flow into capacitor C. Hence the voltage across C will change linearly with time. When S switches back on again, capacitor C will rapidly discharge to practically zero volts.

The actual circuit employed is a slight modification to the one described above. By suitably selecting a resistor in this circuit, small departures from non-linearity in the ramp may be compensated for. Moreover, by using "over compensation," non-linearities in the overall voltage analogue may be minimised. Usually, departures from ramp linearity follow the form depicted in Fig. 12. The percentage departure from linearity increases with time. Expressed analytically

$$\frac{\Delta v}{v} = kt$$

where v is the ramp voltage, t is time, k is the ramp slope

If capacitor C is split to form C_1 and C_2 and a resistor R_C is connected as shown in Fig. 11(b) the following equations apply.

$$i_1 = \frac{V}{R}$$

$$i_2 = \frac{V}{R} + \frac{v_{C1}}{R_C}$$

(where the voltages and currents are as indicated in Fig. 11(b)).

If it is assumed that the capacitors are initially uncharged then the following equations apply.

$$\begin{aligned} v_{C1} &= \frac{1}{C_1}\int_0^t \frac{V}{R}\,dt \\ &= \frac{Vt}{RC_1} \\ v_{C2} &= \frac{1}{C_2}\int_0^t \left(\frac{V}{R} + \frac{Vt}{RR_CC_1}\right)dt \\ &= \frac{Vt}{RC_2} + \frac{Vt^2}{2RR_CC_1C_2} \\ v &= v_{C1} + v_{C2} \\ &= Vt\left(\frac{1}{RC_1} + \frac{1}{RC_2} + \frac{t}{2RR_CC_1C_2}\right) \end{aligned}$$

Putting $C_1 = C_2 = 2C$ we obtain

$$v = \frac{Vt}{RC}\left(1 + \frac{t}{8R_C C}\right)$$

For $R_C = \infty$ the normal linear term only remains. The expression above implies an upward bend in the ideal ramp and can be used to compensate for the tendency of the ramp to droop.

Assume that the ramp requires $x\%$ correction at $t = T$

$$\frac{\Delta v}{v} = \frac{T}{8R_C C} = \frac{x}{100}$$

$$R_C = \frac{12{\cdot}5T}{xC}$$

For example say $x = 2\%$ at $T = 34$ msec, and let $C = 410K$ (picofarad) then

$$R_C = 520K$$

It has been assumed that both capacitors C_1 and C_2 are initially discharged. To ensure that this is the case, it is necessary to add diodes D702 and D703. In the absence of D703, a positive voltage may develop across C703 and, alternatively, in the absence of D702, a negative voltage may be developed.

As the basic ramp is linear to approximately 0·5%, not much compensation is required to linearise the ramp, but to linearise the voltage analogue "over compensation" may be employed.

Ramp voltages appear at both base and emitter of Q702. In the circuit employed (see Fig. 10), the emitter waveform has been used and has been taken off to emitter follower transistor Q703. The emitter follower prevents loading on the ramp generator circuit. In Fig. 13, waveform No. 6 has been redrawn on a different time scale to present a typical data sample of all channels. Negative going ramp waveforms, produced when the output of the gate forming circuit gates Q701 off, have been drawn in waveform No. 7 of Fig. 13. Note that the marker channel produces a ramp height greater than that from any other channel.

For the above discussion, it has been assumed that switch S104 is in the −24 volt position. It will be shown later that in the "auto. cal." position it is possible to perform automatic calibration.

Resistor R706 in Fig. 10 enables the ramp slope to be adjusted over a wide range. A ramp slope of approximately 0·29 volt per millisecond is used.

5.4. Voltage Comparator

The function of the voltage comparator is to provide a synchronising pulse every time a marker pulse arrives. Operation of the comparator circuit may be examined with reference to the circuit diagram of Fig. 14. As the comparator presents a relatively low impedance when triggering occurs, emitter follower Q704 is used to prevent any loading on the ramp input. Loading of the ramp circuit, on triggering of the comparator, is of no embarrassment in the digital system but it may produce marked non-linearity in the analogue output from the marker channel. Under normal conditions the emitter base junction of Q705 is reverse biased and only leakage currents flow. Now the emitter of Q705 follows the negative going ramp voltages of waveform No. 7 in Fig. 13. Prior to triggering, the base of Q705 is held at some negative voltage set by R711. If the magnitude of the negative ramp voltage exceeds the magnitude of the negative voltage on the base of Q705 this transistor will conduct.

For synchronisation purposes, only one pulse each time the marker pulse arrives is required. Hence the triggering level is set between the magnitude of 100% signal ramp and the marker ramp, as illustrated in waveform No. 7 of Fig. 13. With Q705 off, Q706 conducts slightly such that an output of approximately +5 volt appears at T9. When Q705 conducts, Q706 is driven into saturation such that approximately +21 volt appears at T9. Resistor R713 and capacitor C704 provide positive feedback to the base of Q705 to increase the switching speed. A short duration synchronising pulse, as illustrated in waveform No. 8 of Fig. 13, appears at T9 at the end of each marker pulse.

5.5. Synchronised Oscillator

If a signal dropout of sufficient duration occurs during replay of the flight data signal, an additional switching pulse will be generated by the gate forming circuit. Similarly if a random burst of signal appears during an "off" period between data samples, an additional pulse may be

formed by the gate forming circuit. In order that the binary counter (to be described in the next sub-section) may switch in proper synchronism, it is imperative that the counter receive trigger pulses corresponding only to the commencement of data pulses (or, in other words, the leading edges of pulses formed at the output of the gate forming circuit—see waveform No. 6 in Fig. 13). Any additional pulses, formed for the reasons described above, would cause the count to advance in the binary chain if the output from the gate forming circuit were used as the counter trigger source. For example, if a dropout were to occur during the data sample for channel 1, all succeeding samples up to the marker channel (when a counter synchronising pulse is produced) would be gated to the wrong channel.

To virtually eliminate the tendency of the system to temporarily lose synchronism because of the presence of signal dropouts, an astable multivibrator has been incorporated. The untriggered multivibrator free runs at a frequency slightly less than the incoming sampled data rate (24 hertz nominally). In the triggered mode of operation, the multivibrator frequency becomes locked to the incoming sampling rate by way of trigger pulses derived from the output of the gate forming circuit. By making the individual "on" and "off" periods of the free running multivibrator markedly different, an oscillator can be made which is insensitive to trigger pulses except in the region near the start of a data sample. In this way, most of the additional pulses formed because of dropouts or noise pulses cannot upset the counter synchronism.

The complete circuit details of the triggered astable multivibrator circuit are presented in Fig. 15. For the purposes of analysis a simplified circuit, with triggering components omitted, has been drawn in Fig. 16(a). For ease of analysis the zero reference voltage has been taken as the common emitter point in this circuit. The "on" and "off" times of the output waveform will be proportional to R_2C_2 and R_1C_1 respectively. When the transistors revert to the "off" condition, the collectors will not immediately switch to the collector load resistor supply rail, but will rise towards this voltage with recovery time constant R_LC_1 or R_LC_2. For unsymmetrical period operation it is essential to keep the recovery time constant R_LC_2 (in this case the longest) low. The problem arises because the capacitor which affects the recovery time of the short period "off" pulse in the oscillator output (see Fig. 16(c)) is the one associated with the timing of the long period "on" pulse in the oscillator output. In order to minimise the recovery times, R_1 and R_2 are returned to a voltage more negative than the collector supply voltage. In this way the values of R_1 and R_2 may be increased, and hence C_1 and C_2 may be reduced to provide the requisite R_1C_1 and R_2C_2 time constants. By reducing the values of C_1 and C_2 the recovery times may be kept low. Note that R_1 and R_2 must be low enough to provide sufficient current to saturate the transistors in the "on" condition.

A simple analysis of the circuit of Fig. 16(a) enables the period of the free running oscillator to be determined. With Q605 "off" and Q606 "on" C_1 will charge to the collector supply rail voltage. When Q605 is switched on, C_1 will have an initial voltage V_{CC} across its terminals and will begin to discharge with time constant R_1C_1 as illustrated in Fig. 16(b). Referring to this figure we may write:

$$i = \frac{2V_{CC} + v}{R_1}$$

$$v = V_{CC} - \frac{1}{C_1}\int_0^t i\,dt$$

(Note that V_{CC} is the voltage corresponding to initial charge on C_1.)

$$\frac{1}{C_1}\int_0^t i\,dt + iR_1 = 3V_{CC}$$

Differentiating we obtain

$$\frac{i}{C_1} + R_1\frac{di}{dt} = 0$$

Hence $$i = i_0\, e^{-t/(R_1C_1)}$$

where $$i = i_0 \text{ at } t = 0$$

$$i_0 = \frac{3V_{CC}}{R_1}$$

$$i = \frac{3V_{CC}}{R_1}\, e^{-t/(R_1C_1)}$$

$$v = V_{CC}(3e^{-t/(R_1C_1)} - 2)$$

Now when v reaches zero potential approximately, Q606 will switch on and Q605 will switch off. Let $t = T_1$ when $v = 0$

Then $$T_1 = R_1C_1 \, ln \, 1{\cdot}5$$

Similarly $$T_2 = R_2C_2 \, ln \, 1{\cdot}5$$

If T_F is defined as the free running period then

$$T_F = T_1 + T_2$$
$$= (R_1C_1 + R_2C_2) ln \, 1{\cdot}5$$

Further, define T as the nominal period of the data samples (1/24th second).

Due to imperfections in the record/replay system, T will not be absolutely constant but will vary due to recorder wow, pulse width chatter (due to amplitude jitter as outlined in section 5.1), and any drifts in the sampling rate oscillator in the recording unit. If the wire replay and recording speeds differ, an apparent change in sampling rate will result. The synchronised oscillator has been designed such that the absence of 1 trigger pulse (as may occur if a dropout occurs at the start of a sample) in a train of trigger pulses will not desynchronise the system. As the probability that dropouts of sufficiently long duration will occur at the start of 2 consecutive pulses is extremely small, desynchronisation due to this cause will be a rarity.

Let $\pm wT$ be the variation in the nominal period T due to various causes referred to above. Let that part of T, for which the oscillator will respond to start triggers, be denoted by τ (see Fig. 16(c)). For the system to remain in synchronism with 1 of a chain of trigger pulses missing (taking into account the maximum deviation in sampling rate), the following equation applies

$$2T_F - 2T(1 - w) = \tau$$

Put $T_F = T(1 + w)$ (the maximum free running period for the system to run synchronously taking into account the variations in T).

Hence $$\tau = 4wT$$

Allowing for $\pm 3\%$ wow (or record/replay speed variations), $\pm 2\%$ period change due to amplitude chatter and $\pm 1\%$ to cover drift we may put $w = 0{\cdot}06$.

Now $T = \frac{1}{24}$ sec. $= 41{\cdot}7$ msec.

$$T_F = 41{\cdot}7(1 + 0{\cdot}06) \text{ msec.} = 44{\cdot}2 \text{ msec.}$$

$$\tau = 4 \times 0{\cdot}06 \times 41{\cdot}7 \text{ msec.} = 10{\cdot}0 \text{ msec.}$$

It was found experimentally that

$$\tau \simeq 0{\cdot}7T_1$$

Hence T_1 (free running) should be set to 14 msec. C605 has been selected to obtain this value of T_1.

By adjusting R614 (effectively adjusting R_2), T_2 may be adjusted to make $T_F = 44{\cdot}2$ msec.

Positive going start trigger pulses, derived from the output of the gate forming circuit, are diode gated to the base of Q605 to provide oscillator synchronisation. In Fig. 13, waveform No. 9, the oscillator output waveform has been drawn. Note that the "off" going edges of this waveform are somewhat rounded due to the finite recovery time. For this waveform the recovery time constant is R_LC_2 (1·8 msec.).

5.6. Binary Counter

Three symmetrically triggered bistable multivibrators have been cascade connected, as shown in the circuit of Fig. 17, to form a count by 8 binary divider. Positive trigger pulses derived from the output of the synchronised oscillator are diode gated into the first binary. Collector triggering is employed in what is a fairly conventional binary divider.

To allow coupling capacitors C608, C611 and C614 to discharge between trigger pulses, resistors R620, R627 and R634, respectively, have been added.

Under normal conditions, the "off" transistors are reverse biased from either the +24 volt rail via R619, R626 and R633, or from the comparator output (which is nominally +5 volt) via R621, R628 and R635. When a synchronising pulse is generated by the voltage comparator circuit, the voltage at T9 (see Fig. 17) jumps from a nominal +5 volt to approximately +21 volt. The latter voltage is high enough to ensure that transistors Q608, Q610 and Q612 are switched off, if they happen to be in the "on" state when the synchronising pulse arrives. Hence the

synchronising pulse serves to set the counter in a given state (or check that it is in a given state) once every complete cycle of data samples.

In Fig. 18 the various collector waveforms of the binary divider chain have been drawn. The waveforms are shown in relation to the "start" trigger pulses derived from the output of the synchronised oscillator and also the synchronising pulse generated during the sample time of the marker channel (channel 8). As there is a total of 8 channels and a divide by 8 circuit is used, the counter should remain in synchronism (after having been initially synchronised) even in the absence of synchronising pulses. If a signal drop-out occurs during a marker pulse, the ramp output from the ramp generator circuit will be switched back to zero at the time the drop-out arrives and will start from zero again when the drop-out passes. Hence sufficient voltage level will not be reached in the ramp generator output to trigger the voltage comparator, and hence a synchronising pulse will not be generated. For the reasons mentioned above, the absence of the synchronising pulse will not de-synchronise the system. However, should the binary circuit, for any reason, lose synchronism (such as, for example, if the counter is switched to the count 5 state when the channel 4 data sample arrives) the following synchronising pulse, generated when the marker pulse arrives, will restore the synchronism.

Basically, the count by 8 circuit can be employed for any number of channels less than 8. For instance, if a 6 channel system is used, the synchronising pulses will effectively cause the circuit to be reset after the sixth pulse. Under these conditions synchronism depends on the presence of synchronising pulses, and hence, if a drop-out occurs during a marker pulse, the consequent absence of a synchronising pulse will cause the counter to count up to 8. Thus incorrect channel selection will occur until the next synchronising pulse has arrived. This difficulty may be eliminated by the use of feedback diodes to advance the count, if less than 8 channels are employed. If, for instance, 6 channels are used then the basic counter may be converted to a divide by 6 arrangement simply by adding a diode between T15 and T13 (see Fig. 17). Under these conditions the absence of some synchronising pulses will not cause de-synchronisation of the system.

5.7. Channel Selector

Once a binary counter, which switches in synchronism with the incoming data samples, has been designed, it is a simple matter to add a diode "AND" gate which will produce a gate signal associated with any desired channel. If only one channel at a time is to be decoded, a 3 diode "AND" circuit connected to the appropriate binary outputs by means of a selector switch may be conveniently used as the channel selector. Individual channel selection is accomplished within the Electronic Counter (instrument connected externally to the A.R.L. Flight Memory Decoder as illustrated in Fig. 3) by connecting the output of the frequency doubler circuit to the "external frequency standard" terminals and the "AND" circuit gate signal to the "time interval" terminals.

Complete circuit details of the channel selector are presented in Fig. 19. The channel selector switch is shown in the channel 5 position. Each of the binary outputs (T11 to T16) has an "on" level of approximately 0 volt and an "off" level of approximately −21 volt. The 3 deck channel selector switch S103 connects T11, T13 and T16 to the 3 diode "AND" gate in the channel 5 position. If one or more of these outputs is at 0 volt, the output at T17 will be clamped to approximately 0 volt. However, if (and only if) all three outputs are at the "off" potential (−21 volt), diodes D704, D705 and D706 will be reverse biased, and the voltage at T17 will be at approximately −16 volt (taking into account loading effects due to voltage analogue circuit to be discussed later). Note that for the diodes to become reverse biased the potential at T18 must be lower in magnitude than the "off" potential from the binary outputs. For this reason, a zener diode D707 (4·7 volt nominal) has been added as shown in Fig. 19. With the channel selector switch in the No. 5 position a negative going gate signal as revealed in waveform No. 16 of Fig. 18 is generated between the start of the channel 5 data sample and the start of the channel 6 data sample. A similar gate signal is generated about the appropriate data sample, if the channel selector switch is in any other position.

If simultaneous digital presentation of multiple channel information is desired, the single diode "AND" circuit of Fig. 19 may be replaced by a diode matrix. As multiple channel presentation requires the use of multiple counters, the digital presentation system has been confined to a "single channel at a time" presentation.

5.8. Automatic Presentation of Data in Digital Form

Up to date digital presentation of data has been performed using a Type 522B Counter and a Type 562A Digital Recorder, both of Hewlett Packard manufacture. In order to set the Counter for data measurements, the Function Selector Switch is set to "Time Interval," the Time Unit Switch is set to "Ext.", the output of the frequency doubler is connected to the "Ext." input, and the channel selector gate is connected to the "Trigger Input" socket ("Start" and "Stop" connectors joined together). It is to be noted that the gate signal lasts for the duration of a complete data sample period (1/24th second). Hence noise pulses appearing in the signal "off" time may produce additional counts, but as these are a comparative rarity very few errors would be introduced. On the other hand, stopping of the counter would not be produced by short term drop-outs during data pulses (as would be produced if the output of the gate forming circuit were connected to the Trigger Input "Stop" connector and the channel selector gate to the "Start" connector).

Data sample counts appear 3 times per second on the counter for the channel selected. Because of frequency doubling, 100% signal will register as 220 counts and 0% signal as 20 counts. To obtain the value of the sampled parameter, the equivalent zero signal count (20) is subtracted from the count registered and then each count represents 0·5% of maximum signal for the given channel. The digital system described in this paper enables an overall accuracy of $\pm 1\%$ to be obtained, the maximum the system of recording will allow.

For automatic recording of the decoded data in digital form, the Counter may be coupled to the Type 562A Digital Recorder which is quite capable of typing a 3-digit number 3 times per second (actually the 562A is capable of providing 11 columns 5 times per second). In this way consecutive readings appear in rows in the longitudinal direction of the paper tape. To date this form of automatic digital recording has been employed.

Other possibilities come to mind in the field of automatic digital recording of the decoded data signal. For the recording of multiple channels simultaneously, the channel selector may be replaced by a diode matrix and the Counter-Digital Recorder combination may be duplicated for each data channel to be recorded. Such a system would not normally provide correlation between data channels. For automatic recording of the decoded information in serial form on punched paper tape the basic elements required would be—

(1) Electronic Counter (each data channel consecutively gates the counter).
(2) Store (which stores the previous count while the counter counts the pulses from the next data sample).
(3) Parallel to Serial Converter (which converts the parallel information in the store to serial form suitable for driving a tape punch).
(4) High Speed Tape Punch.

A commercial system, which should meet all the requirements for items 2 to 4, is the DY-2545 High Speed Tape Punch Set of Dymec manufacture. This system incorporates—

(1) DY-2545A Tape Punch Coupler (contains information store).
(2) DY-2545B Punch Power Supply.
(3) Teletype BRPE 11 Tape Punch (capable of punching 110 characters/second).

No special problems are involved in choosing a suitable Counter to go with the DY-2545 High Speed Tape Punch Set. Various gating signals and end of line signals (once every complete cycle of data samples) would also be required. In this way all channels may be recorded simultaneously on punched paper tape. Correlation between the readings on various channels is obtained in this system of digital decoding. Subsequently the information on the punched tape may be typed on a typewriter (such as a Flexowriter) or fed to a digital computer for processing.

6. ANALOGUE PRESENTATION OF DATA

Although the digital method of presentation of the flight data provides optimum accuracy ($\pm 1\%$ of full scale), it is not quite as convenient for observing general variations of a parameter throughout a flight as a continuous graphical recording method. For this reason it was considered essential to develop an analogue system of presentation of the demodulated flight data. Numerous methods of producing a suitable analogue signal can be used.

In the system which is used in the decoder, the ramp generator (described in section 5.3) produces a ramp voltage the peak value of which is proportional to the width of the data pulse. By suitable gating of the ramp voltages into peak voltage charging networks a continuous

analogue voltage proportional to the data pulse width is produced for any desired channel. However, as any speed changes occurring between record and playback produce variations in ramp height, the basic system is subject to an error which does not arise in the digital system. Since a zero and a marker (110%) signal are available it is possible to automatically compensate for these errors.

One of the main advantages of this particular system of analogue presentation is that it uses relatively few components and is capable of presenting all channels simultaneously for recording on a multi-channel chart recorder. As a suitable multi-channel chart recorder was not available for use with the decoder at the time of the development of the Ground Station Equipment, only a single analogue channel, as selected by the channel selector switch (described in section 5.7), has been incorporated in the A.R.L. decoder. Laboratory tests carried out using the system of simultaneous decoding of all channels, left no doubt about the feasibility of such a system.

Decoding systems, which produce an analogue voltage signal proportional to the count registered on any particular channel, are inherently free from errors due to speed variations in record and playback of the magnetic wire record. A block schema of a digital to analogue converter, capable of separating one channel of data, is shown in Fig. 20.

For simultaneous presentation of multiple channels, the circuit block of Fig. 20 may be repeated on each desired channel, and the appropriate channel selector gate may be derived from a diode matrix associated with the binary counter described in section 5.6. In operation, the leading edge of the channel selector gate signal resets the counter (capable of counting up to at least 240) and the output of the frequency doubler passes to the counter while the channel selector gate signal is present. If a binary counting system is used, a series of 8 binaries will be required ($2^8 = 256$). If a decade counting system is used, a series of 9 binaries will be required. By summing the currents through resistors of suitably weighted value, connected to the various outputs of the binaries, a staircase type analogue output is generated as the counter counts. The analogue voltage level reached will vary as the number of counts vary. The requisite analogue output will remain stored in the counter until it receives a reset pulse at the commencement of the next data pulse for that channel. As the "count" time is much less than the "store" time, very little filtering of the analogue output signal will be required. For simultaneous presentation of all channels, a total of 8 counters is required (6 for sampled parameter signals and 2 for calibration signals), which requires an appreciable quantity of components.

An alternative system, capable of providing analogue outputs from all channels simultaneously, but requiring only 2 counters, is drawn in the block schema of Fig. 21. In this system one counter counts while the other stores the count registered during the previous data sample. If a single counter only is used, the "dwell" time for the analogue voltage will be dependent on the count duration and hence some non-linearity may result. In the system depicted in Fig. 21, the analogue outputs from the odd number channels are taken from the upper counter and the analogue outputs from the even number channels are taken from the lower counter. The binary circuit performs the necessary switching between the two counters.

Individual channel selection is achieved by using a diode matrix channel selector (associated with the binary counter described in section 5.6) which gates the analogue outputs from the counters to the respective analogue channel outputs during the period for which the analogue output for each channel is stored in the non-counting binary chain. In this way, the analogue output for any channel prior to smoothing is a rectangular waveform lasting for a data sample period (1/24th second). The analogue signals appearing at the output of the channel separator (see Fig. 21) may be gated to a peak charging circuit which provides a continuous analogue output voltage suitable for driving a graphical recorder.

Neither of the systems described in the previous paragraph has been built. Details of the system used in the actual decoder (referred to in the second paragraph of this section) will follow in the next sub-section.

Plotting of the demodulated flight data in analogue form has been performed, one channel at a time, using a Type 581A Digital to Analogue Converter of Hewlett Packard manufacture in conjunction with the Type 522B Counter, referred to in section 5.8 for automatic presentation of flight data in digital form.

6.1. Simple Voltage Analogue

The principle of operation of the voltage analogue may be studied with reference to the simple circuit of Fig. 22. In brief, the circuit charges capacitor C to the peak value of the ramp

voltage of the particular channel selected. As the ramp height is proportional to data pulse width, a voltage signal proportional to the value of the recorded parameter will appear across C. During the period between channel selector gate signals, the voltage at T17 is approximately zero and hence diode D1 will be reverse biased for negative going ramp voltages appearing at T8. When, however, the negative going ramp channel selector gate voltage appears at T17, diode D1 will become forward biased and conduct via R_2. Similarly D2 will now conduct and charging current will flow into C via R_2. If time constant R_2C is relatively short, the voltage across C will follow the ramp voltage at T8. When the channel selector gate signal disappears, both diodes D1 and D2 will become reverse biased and C will discharge with time constant R_1C via R_1. Diodes D1 and D2 will normally conduct only near the peak of the incoming ramp signal as capacitor C discharges to a relatively small extent between successive data samples for the selected channel.

In Fig. 23 a typical voltage analogue signal has been drawn for the circuit of Fig. 22. To prevent loading of the ramp output, R_2 should not be made too small. In the decoder a value of $R_2 = 56K$ has been chosen. For capacitor C to charge at the input signal ramp rate, the required input current is kC where k is the ramp slope (300 volt/sec approximately). At the peak value of ramp voltage (-10 volt approximately) the current through R_2 will be at its minimum value of about 110 microamp. Hence, for the voltage across C to follow the input ramp, C should be less than 0·37 microfarad (110/300). Note that any excess current through R_2, not required for the charging of C, flows via diode D1 through the ramp generator output circuit. When the input ramp voltage returns to zero, the voltage across C will begin to discharge towards zero voltage with time constant R_1C.

The above discharge time constant should be long compared with the repetition period of data samples for a particular channel. As the repetition period of the data samples is $\frac{1}{3}$ second, a figure of $R_1C = 5$ second is suitable. Under these conditions about 7% peak to peak ripple voltage will appear on the basic analogue output voltage. For $C = 0{\cdot}25$ microfarad (less than 0·37 microfarad as required), the required value of R_1 is 20 megohm. Such a resistance figure is quite impractical for most graphical recorders and hence a more complex system employing impedance buffering amplifiers has been used (refer to next section).

For simultaneous analogue decoding of all channels, the simple circuit of Fig. 22 may be repeated for all channels as shown in Fig. 24. In this case the channel selector of Fig. 19 has been replaced by a diode matrix associated with binary outputs T11 to T16. Gate signals appear successively at the various outputs of the diode matrix and analogue voltages associated with the corresponding ramp voltages are formed across the charging capacitors in a similar manner to that described for the single analogue circuit of Fig. 23.

6.2. Practical Voltage Analogue

For the simple circuit of Fig. 22, described in the previous section, there are many undesirable features. It was shown that for capacitor C to charge at the input ramp rate, it should have a value less than 0·37 microfarad approximately. Using a capacitor C of value 0·25 microfarad would mean that a discharge resistor of value 20 megohm would be required to provide a 5-second discharge time constant. Such a value of discharge resistance is very inconvenient. Moreover, the resulting 7% peak to peak ripple is somewhat excessive at 100% signal level. In the simple circuit the rate of discharge of capacitor C, and hence the maximum rate at which the voltage analogue will respond to changes in sampled parameter value, will depend on the analogue signal level. For instance, it would take considerably longer for the analogue output to drop from 20% to 10% value than from, say, 100% to 90% value. To overcome these problems associated with the simple voltage analogue circuit, a more complex circuit as presented in Fig. 25 has been used.

To maintain a relatively long discharge time constant, of the order of some seconds and at the same time reduce the value of the discharge resistor, the diode D2 of the simple circuit of Fig. 22 may be replaced by the transistor Q707 as shown in Fig. 25. In this way capacitor C705, which replaces capacitor C of the simple circuit, may be increased in value. For a common emitter current gain of typically about 25 for transistor Q707, the capacitance as seen at the base of Q707 would be approximately 0·2 microfarad (5M/25). As the voltage drop across forward biased diode D708 and the voltage drop across the forward biased emitter base diode junction of Q707 are approximately equal during charge of C705, the peak voltage at the emitter

of Q707 will be very nearly equal to the peak value of the selected ramp voltage. Variations in the diode voltages due to temperature changes should tend to cancel each other to a large extent in this arrangement.

To enable capacitor C705 to discharge at approximately the same rate over the full range of ramp input voltage, capacitor C705 and associated resistor R722 have been returned to the positive supply line. In this way, capacitor C705 will discharge via R722 towards +24 volt between ramp charging pulses. The time constant of this discharge network is 6·5 second.

If any loading or filtering effect at the emitter of Q707 by way of C706 and R724 is neglected, the performance of the R722–C705 discharge network may be readily evaluated. Assuming that the peak ramp voltage for the marker channel (240 counts) is −10 volt, then the marker analogue voltage appearing at the emitter of Q707 will discharge by about 1·7 volt (17% of maximum analogue signal) to −8·3 volt between successive samples. The equivalent zero signal (20 counts) will discharge from −0·8 volt approximately by 1·2 volt (12% of maximum analogue voltage) to +0·4 volt between ramp pulses. Note that if the voltage on the emitter of Q707 rises to about 0·5 volt the emitter base junction will begin to conduct and the voltage at the emitter of Q707 will become clamped to the zero voltage output at T17 between channel selector gate signals. Under these conditions a marked non-linearity in the analogue output voltage characteristic would result. Although a considerable increase in ripple is produced at the emitter of Q707 over that for the case in which C705 and R722 are returned to common, a significant improvement in the speed of response of the voltage analogue results.

As indicated in the previous paragraph, the ripple appearing on the analogue signal at the emitter of Q707 varies from 17% for the marker signal down to 12% for the "zero" signal (where percentages are expressed with respect to the peak marker channel signal). Obviously such high ripple levels are quite unacceptable in the final analogue output. Now the most significant ripple component is the fundamental, having a frequency of 3 hertz. The ripple is, however, fairly rich in both even and odd harmonics, hence components at 6 hertz, 9 hertz, 12 hertz, etc., appear. To attenuate the fundamental to a very low value, a parallel T notch filter tuned to 3 hertz has been incorporated. The filter comprises components C706, C707, C708, R724, R725 and R726 as shown in Fig. 25. Capacitor C709 provides attenuation of the harmonics of the ripple frequency. Further analogue signal filtering and attenuation is achieved via R727 and the switched damping capacitor bank. As most of the ripple has been attenuated by the time the analogue signal arrives at the damping switch, very little change in analogue signal will result as the amount of damping is varied. The variable damping allows the speed of response of the analogue output to be varied.

The impedance level of the analogue signal appearing at the wiper of the damping switch S102 is quite high (some megohms). To reduce the analogue signal impedance level to a figure which will render the output suitable for most graphical recorders, a triode valve cathode follower is used as an impedance buffer. The attenuation of the analogue signal between the emitter of Q707 and the grid of V701 may be trimmed via R729. Nominally the analogue voltage at the grid of V701 should be approximately 2/3 of the analogue voltage at the emitter of Q707. V701 is a miniature type EC70 triode which operates satisfactorily from the low voltage supplies used for the transistor circuits. It is extremely important that grid current in V701 be kept very low. Since grid current is not likely to be a very stable quantity it will produce a variable shunting effect on the grid resistor (series combination of R728 and R729) which in turn will cause analogue voltage fluctuations at the output. If the error due to grid current is to be kept less than 0·25% of full scale, the grid current variation must be kept below about 0·01 microamp (assuming a 5-volt difference in analogue output between 100% signal and 0% signal). Suitable choice of the plate current in V701 by adjustment of R731 enables the grid current to be reduced below 0·005 microamp.

The cathode follower gain is approximately 0·93 and the output impedance as seen at the analogue output terminal T19 is of the order of a few hundred ohms. If the marker ramp signal is set to approximately −10 volt peak, a swing of about 5 volts in the negative sense should be obtainable at the output as the data input changes from 0% to 100%.

At the time the voltage analogue circuit was designed, the hybrid circuit was considered the simplest method of obtaining the low impedance output. However, it is to be understood that the same function is well within the ambit of semiconductors. An equivalent transistorised buffer amplifier would require more components, both active and passive. As it was envisaged,

at the time of the design of the decoder, that the analogue portion of the data decoder be later extended to provide voltage analogue signals from each channel simultaneously, the additional circuit complexity of a transistorised buffer amplifier represented a slight disadvantage. However, the advent of the field effect transistor to the semiconductor market in recent times would almost certainly mean that a different approach would be used now.

The chart recorder, which has been used most extensively for graphical recording of the analogue outputs, is a single channel potentiometric type having a full scale sensitivity of 10 mV (Speedomax Type). To use such a recorder, the analogue output appearing at T19 is suitably attenuated by the circuit of Fig. 26. Potentiometer R104 provides zero adjustment so that the equivalent "zero" signal may be set to the edge of the chart grid. Adjustment of potentiometer R105 enables 100% signal to be set to a full chart width. In the design of the voltage analogue circuit it was felt that a large amplitude analogue voltage swing (5 volts approximately) at a fairly low impedance level would be capable of driving most graphical recorders which might be used.

Overall voltage analogue output linearity can be readily assessed in the chart recording presented in Fig. 27. In this recording, taken with a Speedomax Recorder, the analogue output has been plotted as a function of data channel count (frequency doubled). "Zero" signal corresponds to 20 counts and 100% signal corresponds to 220 counts. The linearity is approximately 1·5% of full scale. Compensation, using the techniques described in section 5.3, has not been used to date.

It is to be emphasised that the voltage analogue circuit responds more rapidly to an increase in signal than to a decrease. If, due to temporary desynchronisation, a channel of much lower signal reading than the selected channel is wrongly gated into the voltage analogue circuit, very little change in analogue output signal will result, as Q707 will remain off during the presence of the gate signal. On the other hand, if a channel of much higher signal reading than the selected channel is wrongly gated into the voltage analogue circuit, C705 will rapidly charge to the higher signal level, but may take a considerable time (about 2 second if the marker is wrongly connected on to the "zero" channel) to discharge to the normal level corresponding to the channel selected. Hence it is imperative that desynchronisation of the decoder be eliminated as far as possible for proper operation of the voltage analogue circuit.

The armature of switch S105 in Fig. 25 is shown connected to common. For automatic zeroing, to be discussed later, the armature is switched to the "zero" amplifier output T22.

6.3. Automatic Zeroing

Under the conditions specified to date, the voltage analogue signals comprise a "zero" component common to all channels, and a signal component which varies from channel to channel and is proportional to the value of the parameter sampled in the recording process. The "zero" component arises because zero signal is made equivalent to 10 cycles of the 3500 hertz carrier. Automatic zeroing may be performed by subtracting from the normal voltage analogue an appropriate zero signal derived from the channel connected at all times to equivalent zero signal (channel 7).

Let the total voltage analogue signal (average component) appearing on the emitter of Q707 in Fig. 25 be denoted by $e_S + e_Z$ where e_S is the signal component and e_Z is the "zero" component. By voltage divider action, the voltage at the grid of the buffer amplifier stage employing V701 will be some fixed fraction of the average voltage at the emitter of Q707. For simplicity, denote the voltage divider resistors by the symbols R_1 and R_2, where R_1 is the sum of the resistances of R724, R726 and R727, and R_2 is the sum of the resistances of R728 and R729 (see Fig. 25).

The system of automatic zeroing may be studied with reference to the basic schema drawn in Fig. 28. Basically, it is required that the output voltage e_0 from the signal channel voltage analogue be some constant multiplied by e_S. If a separate voltage analogue circuit is produced for the "zero" channel and the output is amplified and fed to the lower end of resistor R_2 of the signal channel voltage analogue, as shown in Fig. 28, then the output e_0 will be given by

$$e_0 = \frac{A_1 R_2}{R_1 + R_2} e_s + \frac{A_1 R_2}{R_1 + R_2}\left(1 + \frac{A_1 A_2 R_1}{R_1 + R_2}\right) e_z$$

where A_1 = buffer amplifier gain (assumed the same for the signal channel voltage analogue and the "zero" channel voltage analogue) and A_2 = "zero" amplifier gain.

If

$$1 + \frac{A_1 A_2 R_1}{R_1 + R_2} = 0$$

$$e_0 = \frac{A_1 R_2}{R_1 + R_2} e_s$$

which is of the form required.

Hence the requisite gain of the zero amplifier is given by

$$A_2 = -\frac{1}{A_1}\left(1 + \frac{R_2}{R_1}\right)$$

The buffer amplifier gain A_1 is approximately unity and R_2/R_1 is approximately 2.

Hence $A_2 \simeq -3$.

The zero channel voltage analogue, referred to in Fig. 28, uses a circuit virtually identical to the one used for the signal channel voltage analogue drawn in Fig. 25, except that no adjustable components are incorporated. Complete circuit details of the zero channel voltage analogue are given in Fig. 29. Gating of the zero channel ramp is achieved by permanently connecting diodes D802, D803 and D804 to the binary outputs T11, T14 and T16 respectively in an "AND" circuit arrangement. The zero channel analogue output appears at T20 relatively ripple free.

The circuit of the "zero" amplifier, referred to in Fig. 28, is presented in Fig. 30. The gain of the amplifier is feedback stabilized to a figure of approximately −3. Settting of the gain is performed by adjustment of potentiometer R902, which changes the ratio of the feedback resistor value (value of R901 plus associated portion of R902) to the input resistor value (value of R903 plus associated portion of R902). When the gain has been appropriately adjusted, the zero may be set by adjustment of R910. In other words, R910 is set such that zero output is obtained with zero input.

6.4. Automatic Calibration

The provision of a marker channel, which is connected to a fixed D.C. potential in the recording equipment, enables all channels to be calibrated. Any speed changes between record and replay of the data signal will effectively produce pulse duration changes in the data signal. Such changes, in turn, will produce changes in the analogue output. During record and playback of the wire recording, the head moves up and down vertically, with a repetition period of approximately 15 second, in such a manner that the wire winds evenly on or off the spools. At times a noticeable wow component having a repetition period equal to that of the head traverse (15 second) appears on the analogue signals. As such speed variations produce proportional variations in the analogue output from each channel, it is possible to compensate for the variations on the signal channels by observing the variation on the marker channel. In the system to be described here variations in the analogue output due to speed variations between record and replay of the wire recording are cancelled out to a large extent in a system of automatic calibration.

The basic principle of automatic calibration may be studied with reference to the block schema of Fig. 31. Due to difficulties encountered with hunting in a completely closed loop automatic calibrating system, such a system was abandoned. The system used employs a separate ramp generator and voltage analogue circuit for extracting the marker analogue signal. Variations in the marker analogue signal, due to causes outlined in the previous paragraph, will be inherent in the output signal from the marker voltage analogue. The output from the marker voltage analogue is compared with a fixed D.C. reference and the difference is amplified and fed back to the signal ramp generator in such a way as to cause the slope of the signal ramp to vary. By suitable selection of the differential amplifier gain the correct amount of compensation may be established.

Consider that, due to speed variations between record and playback, the width of the data pulses is increased by a fraction ε. To assist in the analysis the various signal levels throughout the automatic calibration circuit have been presented in the block diagram of Fig. 31 for a fractional increase in data pulse width of ε. If T_c is the normal width of the marker pulse, then, the input to the marker ramp generator may be written as $T_c(1 + \varepsilon)$. The analogue voltage appearing at the output of the marker voltage analogue may be written as $K_1 T_c(1 + \varepsilon)$ where K_1 is a constant depending on marker ramp slope and attenuation within the marker voltage analogue circuit. If the reference side of the differential amplifier is fed with the normal output voltage

K_1T_c, then an output signal proportional to ε, actually $\varepsilon\beta K_1T_c$, will be obtained from the differential amplifier where β is the differential amplifier gain. Now the slope of a ramp generator is proportional to the D.C. supply voltage. By subtracting the output of the differential amplifier from the ramp supply voltage V_{cc} and feeding the difference voltage to the signal ramp generator, variation in the signal ramp slope is accomplished. Assume that the signal voltage analogue is separating a channel of input pulse width nominally T but changed to $T(1 + \varepsilon)$ on account of a speed variation. The output voltage of the signal ramp generator circuit may then be written as $K_2(V_{cc} - \beta\varepsilon K_1T_c)T(1 + \varepsilon)$ where K_2 is some constant depending on the passive components in the ramp generator circuit.

Assuming that the nominal "zero" pulse has a width of T_0, then, by virtue of the speed variation, this width will be changed to $T_0(1 + \varepsilon)$. If automatic zeroing is used in the signal voltage analogue circuit the final output will be given by

$$e_0 = K_3(V_{cc} - \beta\varepsilon K_1T_c)(T - T_0)(1 + \varepsilon)$$

where K_3 is a constant depending on the value of K_2 and the attenuation within the voltage analogue circuit.

If βK_1T_c is made equal to V_{cc}, or in other words β is made equal to $\frac{V_{cc}}{K_1T_c}$ the following expression applies for e_0.

$$\begin{aligned} e_0 &= K_3V_{cc}(1 - \varepsilon)(T - T_0)(1 + \varepsilon) \\ &= K_3V_{cc}(T - T_0)(1 - \varepsilon^2) \end{aligned}$$

If ε is, say, a 5% variation then the error produced in this automatic compensating system will be reduced to ε^2 or 0·25%.

The circuit of the marker ramp generator is drawn in Fig. 32. It is very similar to the signal ramp generator drawn in Fig. 10 and described in section 5.3. To prevent loading on the basic ramp generator circuit the output is taken via an emitter follower to the marker channel voltage analogue circuit drawn in Fig. 33. Marker channel (channel 8) gating diodes D806, D807 and D808 are permanently connected to the appropriate binary circuit outputs such that the marker channel is separated. Analogue signal attenuation and ripple filtering is virtually identical to that described for the signal voltage analogue circuit in section 6.2. The marker analogue voltage output, appearing at T21 in the marker channel voltage analogue circuit of Fig. 33, is fed to one side of the differential amplifier shown in Fig. 34. The other side of this differential amplifier is connected to a fixed D.C. reference and is adjusted via R918 to the normal output from the marker channel voltage analogue. The difference voltage is amplified by the differential stage comprising transistors Q907 and Q908. Coupling to the amplifier output by way of a pair of emitter followers, Q909 and Q910, enables a low impedance output, suitable for feeding to the signal ramp generator circuit, to be obtained. Since Q909 and Q910 are NPN and PNP types respectively any changes in emitter base voltage due to temperature variations will tend to cancel to a large extent. The output of the marker amplifier is returned to the signal ramp generator of Fig. 10 via the Auto-Cal. switch S104.

In Fig. 35 the marker channel output as derived from the signal voltage analogue circuit has been compared for the case of the automatic calibration operative and inoperative. Most of the low frequency wow component (having a repetition period of 15 second approximately) disappears with the automatic calibration operative.

The overall accuracy obtainable using the analogue system of decoding is $\pm 2\%$ of full scale. By virtue of the recording system employed, the maximum accuracy obtainable with any decoding method is $\pm 1\%$ full scale (or possibly $\pm 0{\cdot}5\%$ under ideal conditions).

7. POSSIBLE FUTURE EXTENSIONS AND MODIFICATIONS TO THE DATA DECODER

The present decoder has been designed for an 8-channel system employing a sampling rate of 24 per second. If the sampling rate and the data carrier frequency (3500 hertz) were left unchanged and the number of channels were increased, very little modification would be required on the present decoder. The binary counter and the channel selector, described in sections 5.6 and 5.7 respectively, would be changed a little. By adding one additional bistable circuit to the binary chain and an additional section to the channel selector switch, up to 16 channels of data

could be handled. As a change in the number of channels under these conditions would mean a different sampling rate for an individual channel, some alteration would be required in the voltage analogue filter circuits. For the sampling rate to be increased, the data carrier frequency would also have to be increased to maintain the same accuracy. To record a higher data frequency a higher wire speed would be required. For increased data sampling rate the resulting circuit differences in the Ground Station Equipment would be a new flight data band pass filter tuned to the new data carrier frequency and a decoder with slightly modified timing and analogue voltage filtering circuits.

Extension of the voltage analogue portion of the decoder for simultaneous graphical presentation of multiple channels is a relatively straightforward matter. A voltage analogue circuit of the form drawn in Fig. 25 would be required for each channel. In addition, the present channel selector circuit would have to be replaced by a diode matrix. Although more complex, a voltage analogue circuit employing a counter and a digital to analogue converter (see introductory portion of section 6) would have considerable advantage over the present system. Errors due to speed variations between record and playback would not arise. Automatic zeroing and calibration could be readily incorporated in such a system of analogue voltage generation.

If a speed difference exists between record and playback of the magnetic wire record, the time scale as presented on a graphical recorder (recording the voltage analogue signal) will not be correct. To overcome this problem, it would be advantageous to derive timing signals from the actual recording. If the 24 hertz oscillator used in connection with the solid state sampling switch in the Airborne Recording Unit has a high degree of frequency stability it may be used during decoding of records as an elapsed time reference. Since the counter chain described in section 5.6 divides by 8, a nominal 3 hertz signal is available. If a series of frequency dividers were used timing pips at, say, 1 minute intervals (divide by 180) could be put on the chart record.

8. CONCLUSION

(a) The flight data decoder has been successfully used as part of the Ground Station Equipment for decoding records taken in flight using the A.R.L. Flight Memory Airborne Equipment.

(b) Automatic digital or analogue presentation of the flight data is possible if the Ground Station Equipment is coupled to an electronic counter or a chart recorder respectively.

(c) The flight data decoder has been designed to minimize the effects of amplitude dropouts inherent in the record/replay process.

(d) The overall accuracy obtainable with the digital system of presentation is $\pm 1\%$ and that obtainable with the analogue system of presentation is $\pm 2\%$.

(e) By using a more sophisticated analogue system errors due to static or time varying speed differences between record and replay can be largely eliminated and automatic calibration can be performed.

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Author	Title
1. K. F. Fraser	Ground Station Equipment for Decoding the Recordings of a Flight Recorder. A.R.L. Instr. Report No. 26.
2. K. F. Fraser	Response of a Band Pass Filter with Maximally Flat Amplitude Characteristic to a Suddenly Applied Sinusoidal Voltage. A.R.L. Instr. Note No. 70.
3. D. A. Williams	Transistors Ruggedize Airborne Telemetry Keyer. Electronics, Vol. 31, No. 37, September 12, 1958.

APPENDIX

Certain types of components occur so often that a full description will not be repeated in each case. The following abbreviations will be made:

D.C.C.—Resistor, fixed, I.R.C. Type D.C.C., deposited carbon, $\frac{1}{2}$ watt, 1%, high stability.

RC7K—Resistor, fixed, composition, RC7K (Services classification), $\frac{1}{4}$ watt.

POLYESTER—Capacitor, fixed, polyester dielectric, Philips Type C296.

All resistance values are given in ohms (K = 10^3 and M = 10^6).

All capacitance values are given in picofarads (K = 10^3 and M = 10^6). Thus 1K ≡ 0·001 microfarad and 1M ≡ 1 microfarad.

The various components have been given an identification consisting of a letter plus three digits. The letter serves to identify the class of component as summarised in the table below.

Letter Identification	Class of Component
R	Resistor
C	Capacitor
L	Inductor or Transformer
D	Diode
Q	Transistor
V	Valve
P	Plug, Socket or Connector
S	Switch

As regards the number identification, the first number in each case signifies the chassis number and the last two serve to identify the component within that chassis. Thus R612 means resistor No. 12 on chassis No. 6.

The chassis numbering is related to the various modules which make up the A.R.L. Flight Memory Ground Station Equipment as follows:

Chassis No.	Description
1	Front panel
2	Power supply module
3	Speech channel module
4	Panel A plug-in—Pre-amplifier, First Stage of Flight Data Filter
5	Panel B plug-in—Second Stage of Flight Data Filter, A.G.C. Circuit.
6	Panel C plug-in—Frequency Doubler, Synchronised Oscillator, Binary Counter
7	Panel D plug-in—Ramp Generator, Voltage Comparator, Signal Voltage Analogue
8	Panel E plug-in—Zero and Calibrate Voltage Analogues
9	Panel F plug-in—Auto-calibration Circuits

For a more comprehensive description of Ground Station hardware Reference 1 should be consulted. Chassis 2, 3 and 4, and parts of 1 and 5, are detailed in Reference 1. Complete component details are given for chassis 1 and 5 although some of the components do not appear in this text.

CHASSIS No. 1

Legend	Value	Description
R101	10K	Resistor, variable, wire wound, I.R.C. Type W, 1 watt
R102	5K	Resistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
R103	250	Rsesistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
R104	10K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R105	500	Resistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
C101	1000M	Capacitor, electrolytic, Hunts, 50 V.W.
P101		Socket, Cannon Type DA-15S
P102		Socket, valve, 9 pin, mica loaded, Teletron Type ST29L
P103		Socket, miniature, Teletron Type SS24
P104		Socket, Cannon Type DA-15S
P105		Socket, Cannon Type DB-25S
P106		Socket, Cannon Type DB-25S
P107		Socket, Cannon Type DB-25S
P108		Socket, Cannon Type DA-15S
P109		Socket, Cannon Type DA-15S
P110		Jack, panel, Bulgin Type J6
P111		Socket, Banana, 4 mm, Belling Lee Type L1318, red
P112		Socket, Banana, 4 mm, Belling Lee Type L1318, black
P113		Socket, Banana, 4 mm, Belling Lee Type L1318, red
P114		Socket, Banana, 4 mm, Belling Lee Type L1318, red
P115		Socket, Banana, 4 mm, Belling Lee Type L1318, black
P116		Socket, Banana, 4 mm, Belling Lee Type L1318, black
P117		Socket, Banana, 4 mm, Belling Lee Type L1318, red
P118		Socket, Banana, 4 mm, Belling Lee Type L1318, red
P119		Socket, 4 pin, Painton No. 310035 (chassis mounting)
P120		Socket, co-axial, Belling Lee Type L734/S
P121		Socket, co-axial, Belling Lee Type L734/S
S101		Switch, Oak, non-shorting, bakelite, 1 deck, 1 pole, 11 position
S102		Switch, Oak, non-shorting, bakelite, 1 deck, 1 pole, 11 position
S103		Switch, Oak, non-shorting, bakelite, 3 deck, 1 pole, 11 position
S104		Switch, toggle, double pole, change over, Bulgin S270PD
S105		Switch, toggle, double pole, change over, Bulgin S270PD
S106		Switch, toggle, double pole, change over, Bulgin S270PD
S107		Switch, toggle, double pole, change over, Bulgin S270PD
S108		Switch, Palec, non-shorting, bakelite, 2 deck, 1 pole, 12 position
S109		Switch, Oak, non-shorting, bakelite, 1 deck, 2 pole, 5 position
S110		Switch, Palec, non-shorting, bakelite, 2 deck, 1 pole, 12 position

CHASSIS No. 5

Legend	Value	Description
R501	8.2K	D.C.C.
R502	20K	D.C.C.
R503	4.7K	D.C.C.
R504	2.4K	D.C.C.
R505	2.4K	D.C.C.
R506	1.2K	D.C.C.
R507	5.1K	D.C.C.
R508	620	D.C.C.
R509	180K	D.C.C.
R510	10K	RC7K, 10%
R511	2.2K	RC7K, 10%
R512	100K	D.C.C.
R513	47K	D.C.C.
R514	5.6K	RC7K, 10%
R515	15K	D.C.C.
R516	4.7K	D.C.C.
R517	120K	D.C.C.
R518	4.7K	D.C.C.
R519	270	D.C.C.
R520	15K	D.C.C.
R521	270	D.C.C.
R522	8.2K	D.C.C.
R523	27K	RC7K, 10%
R524	10K	D.C.C.
R525	4.7K	D.C.C.
R526	22K	RC7K, 10%
C501	39K	Polyester, 400 V.W., 1% (by selection)
C502	18.8K	(12K + 6.8K) Polyester, 400 V.W., 1%
C503	18.8K	(12K + 6.8K) Polyester, 400 V.W., 1%
C504	45K	(27K + 18K) Polyester, 400 V.W., 1%
C505	5M	Capacitor, fixed, electrolytic, Ducon Type ES, 75 V.W.
C506	25M	Capacitor, fixed, electrolytic, Ducon Type ES, 25 V.W.
C507	10K	Polyester, 400 V.W.
C508	25M	Capacitor, fixed, electrolytic, Ducon Type ES, 25 V.W.
C509	470K	Polyester, 125 V.W.
C510	100M	Capacitor, fixed, electrolytic, Ducon Type ES, 12 V.W.
D501		Diode, germanium, Type OA95
Q501		Transistor, germanium, Type OC77
Q502		Transistor, germanium, Type OC77
Q503		Transistor, germanium, Type OC77
Q504		Transistor, germanium, Type OC77
Q505		Transistor, germanium, Type OC77
Q506		Transistor, germanium, Type OC77

CHASSIS No. 6

Legend	Value	Description
R601	10K	RC7K, 10%
R602	10K	RC7K, 10%
R603	10K	RC7K, 10%
R604	2.5K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R605	390K	RC7K, 10%
R606	3.9M	RC7K, 10%
R607	10K	RC7K, 10%
R608	150K	RC7K, 5%
R609	390K	RC7K, 5%
R610	18K	RC7K, 10%
R611	22K	D.C.C.
R612	1.8M	RC7K, 10%
R613	1M	D.C.C.
R614	500K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R615	680K	D.C.C.
R616	22K	D.C.C.
R617	6.8K	RC7K, 5%
R618	68K	RC7K, 5%
R619	270K	RC7K, 5%
R620	100K	RC7K, 5%
R621	47K	RC7K, 5%
R622	68K	RC7K, 5%
R623	6.8K	RC7K, 5%
R624	6.8K	RC7K, 5%
R625	68K	RC7K, 5%
R626	270K	RC7K, 5%
R627	100K	RC7K, 5%
R628	47K	RC7K, 5%
R629	68K	RC7K, 5%
R630	6.8K	RC7K, 5%
R631	6.8K	RC7K, 5%
R632	68K	RC7K, 5%
R633	270K	RC7K, 5%
R634	100K	RC7K, 5%
R635	47K	RC7K, 5%
R636	68K	RC7K, 5%
R637	6.8K	RC7K, 5%
C601	1K	Polyester, 400 V.W.
C602	47K	Polyester, 125 V.W.
C603	1K	Polyester, 400 V.W.

Legend	Value	Description
C604	470	Capacitor, fixed, polystyrene dielectric, Ducon Styroseal Type DFB
C605	39K	Polyester, 125 V.W. (selected value)
C606	82K	Polyester, 125 V.W.
C607	1K	Polyester, 400 V.W.
C608	1K	Polyester, 400 V.W.
C609	1K	Polyester, 400 V.W.
C610	1K	Polyester, 400 V.W.
C611	1K	Polyester, 400 V.W.
C612	1K	Polyester, 400 V.W.
C613	1K	Polyester, 400 V.W.
C614	1K	Polyester, 400 V.W.
C615	1K	Polyester, 400 V.W.
L601		Transformer, Fortiphone, Type MM1A
D601		Diode, germanium, Type OA95
D602		Diode, germanium, Type OA95
D603		Diode, germanium, Type OA95
D604		Diode, germanium, Type OA95
D605		Diode, germanium, Type OA95
D606		Diode, germanium, Type OA95
D607		Diode, germanium, Type OA95
D608		Diode, germanium, Type OA95
D609		Diode, germanium, Type OA95
D610		Diode, germanium, Type OA95
Q601		Transistor, germanium, Type OC77
Q602		Transistor, germanium, Type OC77
Q603		Transistor, germanium, Type OC77
Q604		Transistor, germanium, Type OC77
Q605		Transistor, silicon, Type OC205
Q606		Transistor, silicon, Type OC205
Q607		Transistor, germanium, Type OC77
Q608		Transistor, germanium, Type OC77
Q609		Transistor, germanium, Type OC77
Q610		Transistor, germanium, Type OC77
Q611		Transistor, germanium, Type OC77
Q612		Transistor, germanium, Type OC77

CHASSIS No. 7

Legend	Value	Description
R701	22K	D.C.C.
R702	390K	D.C.C.
R703	1K	RC7K, 10%
R704	10K	RC7K, 10%
R705		Compensating Resistor—Value to be Selected—D.C.C.
R706	250K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R707	100K	D.C.C.
R708	100K	RC7K, 10%
R709	100K	RC7K, 10%
R710	10K	D.C.C.
R711	10K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R712	10K	D.C.C.
R713	100K	RC7K, 10%
R714	4.7K	RC7K, 10%
R715	330K	RC7K, 10%
R716	12K	RC7K, 10%
R717	4.7K	RC7K, 10%
R718	470	RC7K, 10%
R719	10K	RC7K, 10%
R720	8.2K	RC7K, 10%
R721	56K	RC7K, 10%
R722	1.3M	D.C.C.
R723	4.7K	RC7K, 10%
R724	510K	D.C.C.
R725	255K	D.C.C. (made from two 510K's in parallel)
R726	510K	D.C.C.
R727	510K	D.C.C.
R728	2.7M	D.C.C.
R729	500K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R730	15K	RC7K, 5%
R731	50K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R732	100K	D.C.C.
C701	100M	Capacitor, fixed, electrolytic, Ducon Type ET, 25 V.W.
C702	820K	Polyester, 125 V.W.
C703	820K	Polyester, 125 V.W.
C704	220	Capacitor, fixed, polystyrene dielectric, Ducon Styroseal Type DFB
C705	5M	Capacitor, fixed, electrolytic, Stantelum, 50 V.W.
C706	102K	Polyester, 125 V.W., 1% selected value
C707	204K	Polyester, 125 V.W., 1% selected value
C708	102K	Polyester, 125 V.W., 1% selected value
C709	150K	Polyester, 125 V.W.
C710	100K	Polyster, 125 V.W.
C711	220K	Polyester, 125 V.W.
C712	470K	Polyester, 125 V.W.
C713	1M	Polyester, 125 V.W.

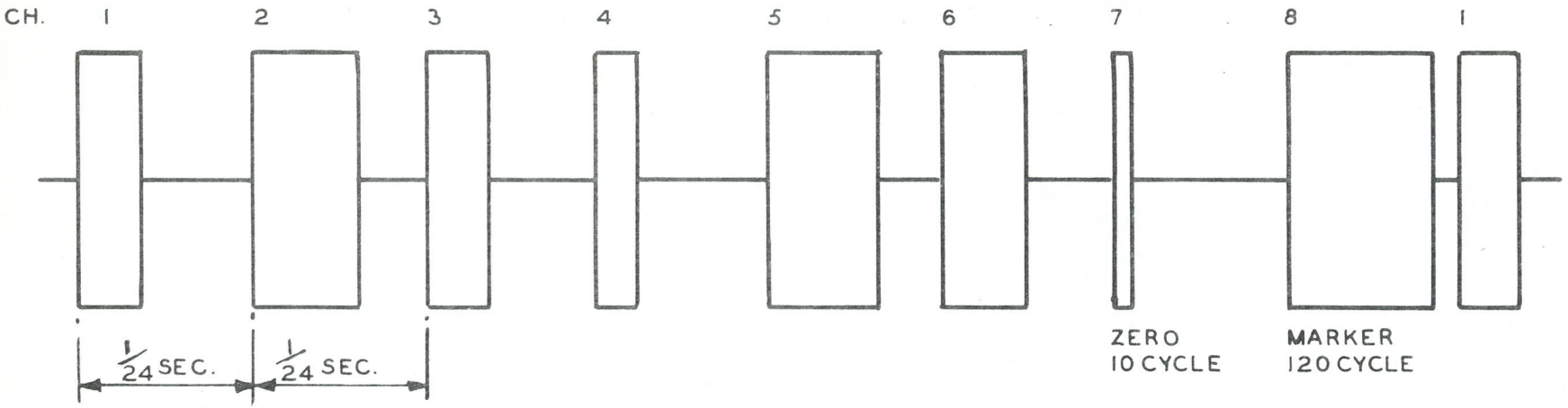
Legend	Value	Description
D701		Diode, silicon, Type OA200
D702		Diode, silicon, Type OA200
D703		Diode, silicon, Type OA200
D704		Diode, silicon, Type OA200
D705		Diode, silicon, Type OA200
D706		Diode, silicon, Type OA200
D707		Diode, silicon, Zener, Type Z2A47
D708		Diode, silicon, Type OA200
Q701		Transistor, silicon, Type BCZ11
Q702		Transistor, silicon, Type BCZ11
Q703		Transistor, silicon, Type 2N335
Q704		Transistor, germanium, Type OC77
Q705		Transistor, germanium, Type 2T64
Q706		Transistor, germanium, Type OC77
Q707		Transistor, silicon, Type BCZ12
V701		Valve, triode, Type EC70

CHASSIS No. 8

Legend	Value	Description
R801	10K	RC7K, 10%
R802	56K	RC7K, 10%
R803	1.3M	D.C.C.
R804	4.7K	RC7K, 10%
R805	510K	D.C.C.
R806	255K	D.C.C. (made from two 510K's in parallel)
R807	510K	D.C.C.
R808	510K	D.C.C.
R809	3M	D.C.C.
R810	100K	RC7K, 10%
R811	10K	RC7K, 10%
R812	56K	RC7K, 10%
R813	1.3M	D.C.C.
R814	4.7K	RC7K, 10%
R815	510K	D.C.C.
R816	255K	D.C.C. (made from two 510K's in parallel)
R817	510K	D.C.C.
R818	510K	D.C.C.
R819	3M	D.C.C.
R820	47K	RC7K, 10%
R821	4.7	Resistor, fixed, composition, RC7H (Services classification), $\frac{1}{2}$ watt
R822	4.7K	D.C.C.
R823	4.7K	D.C.C.
C801	5M	Capacitor, fixed, electrolytic, Stantelum, 50 V.W.
C802	102K	Polyester, 125 V.W., 1% selected value
C803	204K	Polyester, 125 V.W., 1% selected value
C804	102K	Polyester, 125 V.W., 1% selected value
C805	150K	Polyester, 125 V.W.
C806	1M	Polyester, 125 V.W.
C807	5M	Capacitor, fixed, electrolytic, Stantelum, 50 V.W.
C808	102K	Polyester, 125 V.W., 1% selected value
C809	204K	Polyester, 125 V.W., 1% selected value
C810	102K	Polyester, 125 V.W., 1% selected value
C811	150K	Polyester, 125 V.W.
C812	100K	Polyester, 125 V.W.
D801		Diode, silicon, Type OA200
D802		Diode, silicon, Type OA200
D803		Diode, silicon, Type OA200
D804		Diode, silicon, Type OA200
D805		Diode, silicon, Type OA200
D806		Diode, silicon, Type OA200
D807		Diode, silicon, Type OA200
D808		Diode, silicon, Type OA200
Q801		Transistor, silicon, Type BCZ12
Q802		Transistor, silicon, Type BCZ12
V801		Valve, triode, Type EC70
V802		Valve, triode, Type EC70

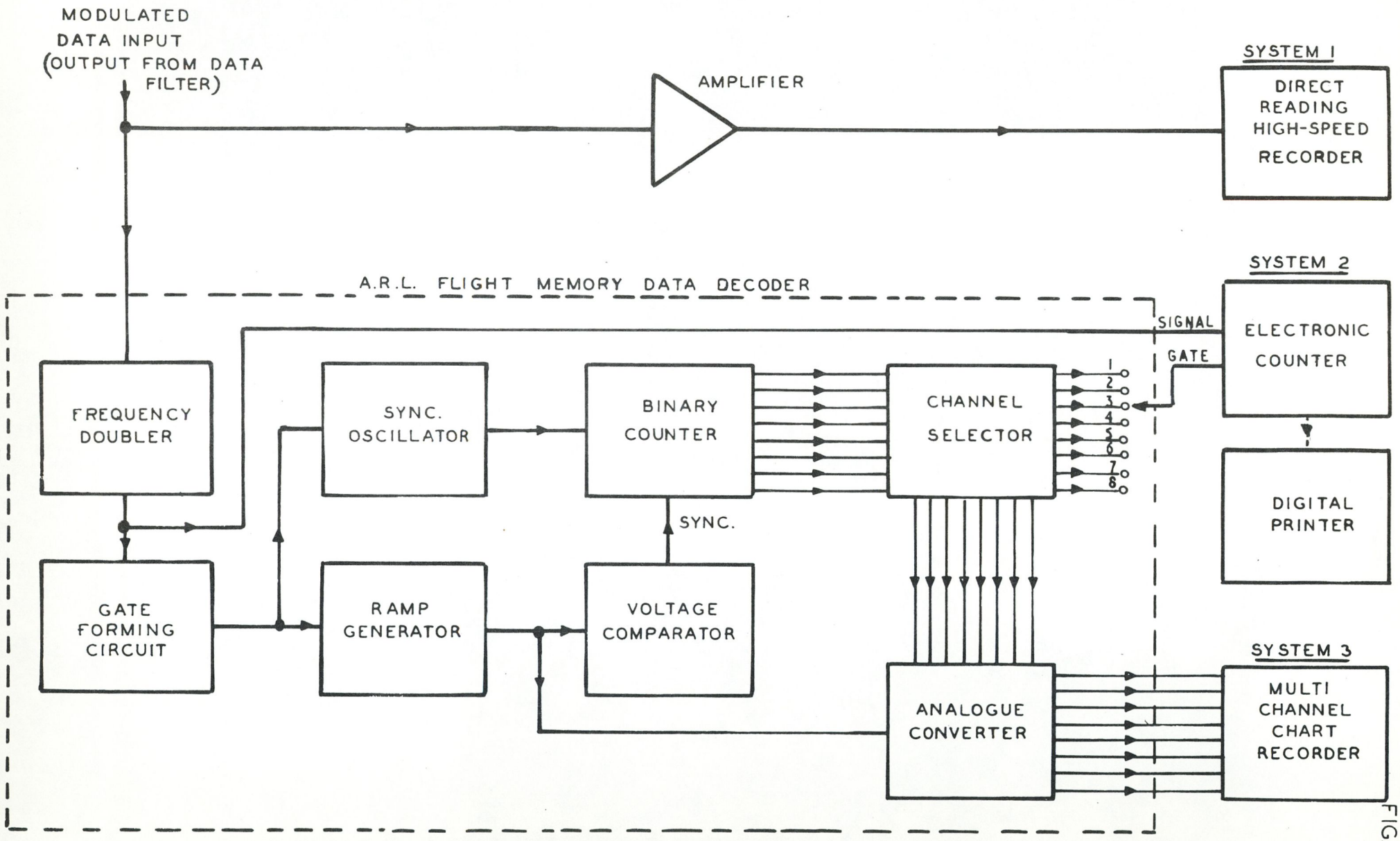
CHASSIS No. 9

Legend	Value	Description
R901	68K	D.C.C.
R902	2K	Resistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
R903	22K	D.C.C.
R904	4.7K	D.C.C.
R905	18K	D.C.C.
R906	330K	D.C.C.
R907	56K	D.C.C.
R908	220K	D.C.C.
R909	4.7K	D.C.C.
R910	1K	Resistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
R911	4.7K	D.C.C.
R912	1K	RC7K, 10%
R913	10K	RC7K, 10%
R914	250K	Resistor, variable, composition, linear, Morganite Type BJ, 0.1 watt
R915	100K	D.C.C.
R916	100K	RC7K, 10%
R917	3.9K	D.C.C.
R918	1K	Resistor, variable, wire wound, Colvern Type CLR 1106/22, 1 watt
R919	1K	D.C.C.
R920	510	D.C.C.
R921	15K	D.C.C.
R922	510	D.C.C.
R923	3.9K	D.C.C.
R924	3.9K	RC7K, 10%
R925	1K	RC7K, 10%
R926	10K	RC7K, 10%
C901	100M	Capacitor, fixed, electrolytic, Ducon Type ET, 25 V.W.
C902	470K	Polyester, 125 V.W.
D901		Diode, silicon, Type OA200
Q901		Transistor, germanium, Type OC77
Q902		Transistor, silicon, Type 2N338
Q903		Transistor, silicon, Type 2N338
Q904		Transistor, silicon, Type BCZ11
Q905		Transistor, silicon, Type BCZ11
Q906		Transistor, silicon, Type 2N333
Q907		Transistor, silicon, Type BCZ11
Q908		Transistor, silicon, Type BCZ11
Q909		Transistor, silicon, Type 2N338
Q910		Transistor, silicon, Type OC201



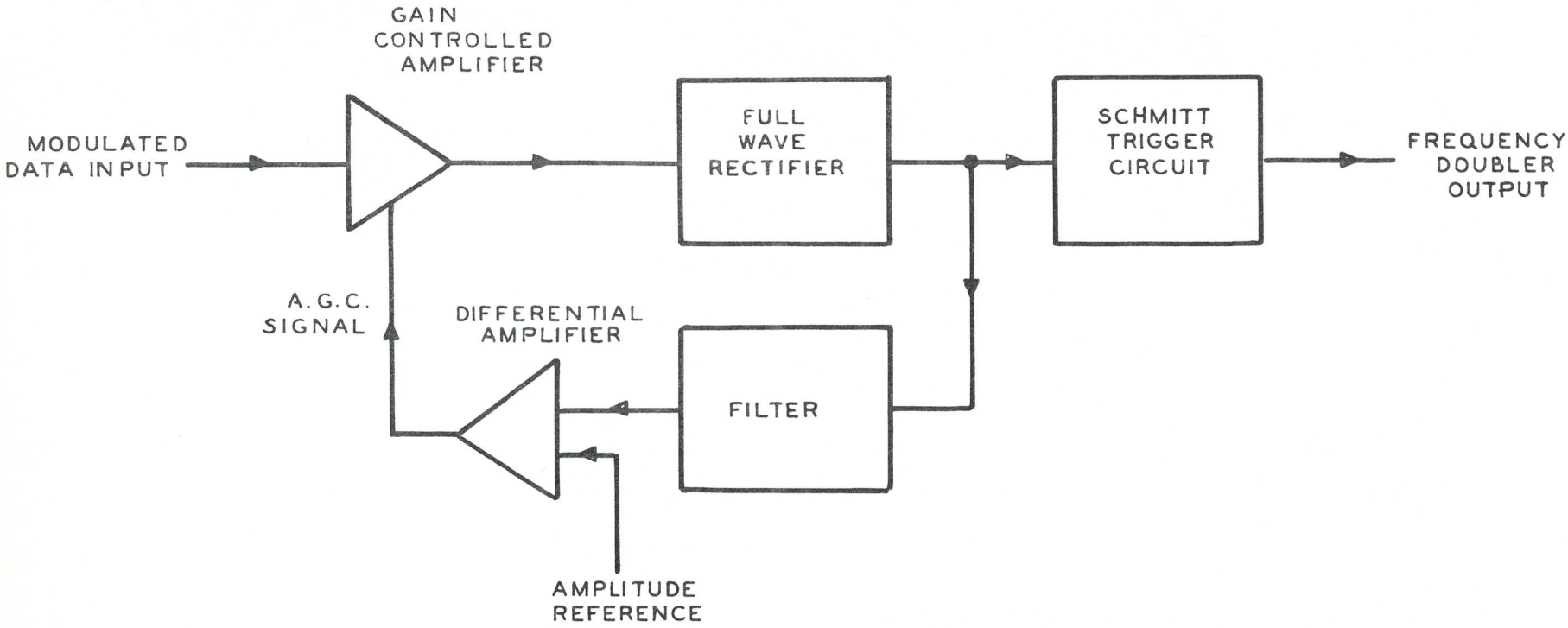
ENVELOPES OF RECORDED DATA SIGNAL (3500 HERTZ SINEWAVE BURSTS)

INST. REPORT 25
FIG. 1



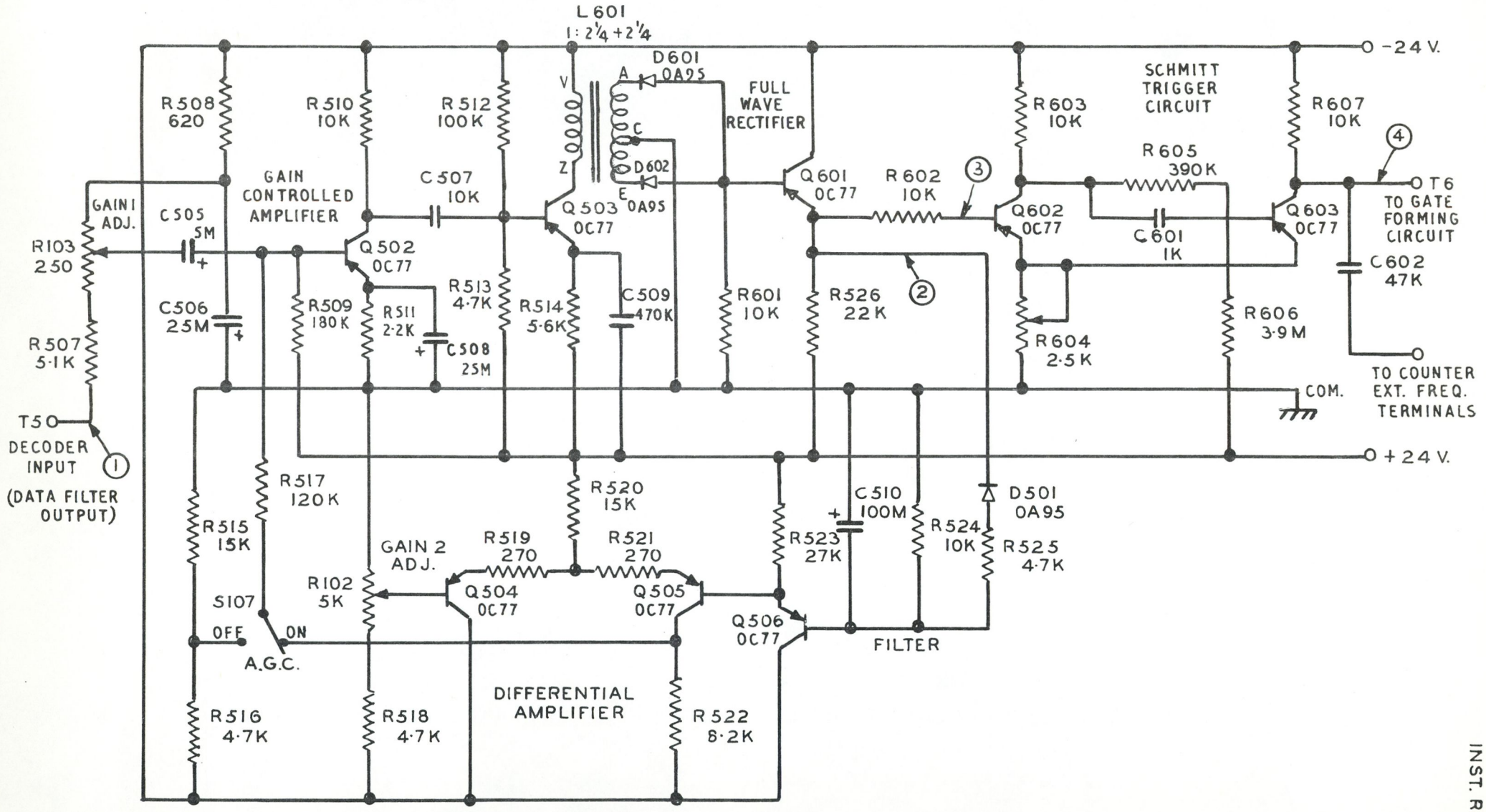
BLOCK SCHEMA OF VARIOUS SYSTEMS OF FLIGHT DATA DECODING

INST. REPORT 25
FIG. 3



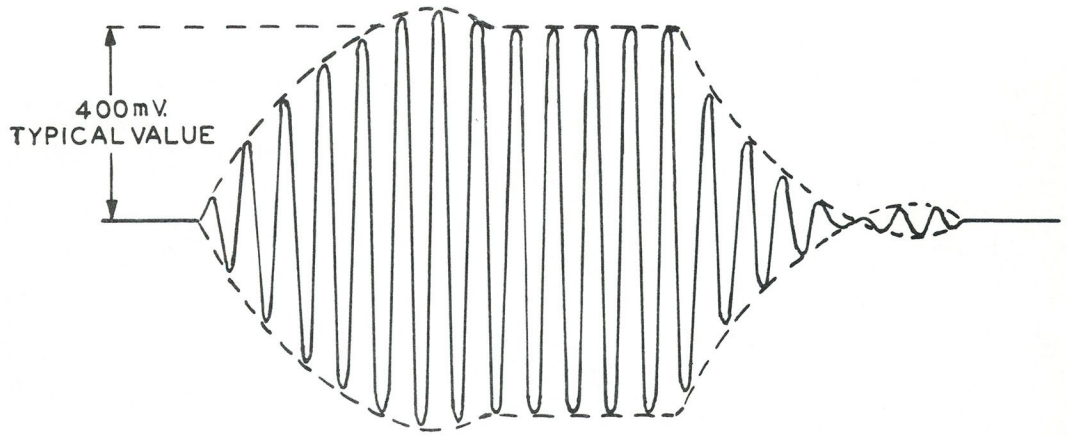
FREQUENCY DOUBLER BLOCK SCHEMA

INST. REPORT 25
FIG. 4

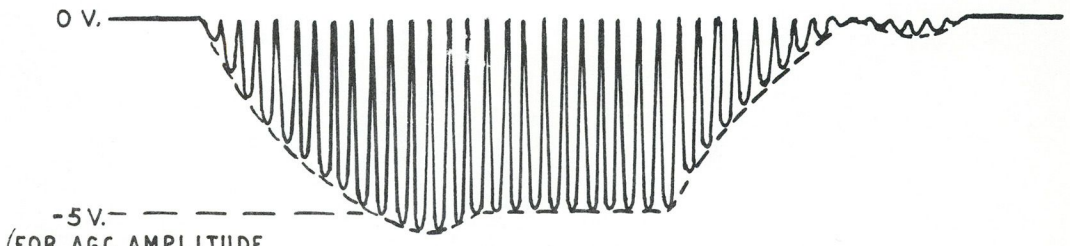


FREQUENCY DOUBLER AND ASSOCIATED CIRCUITS

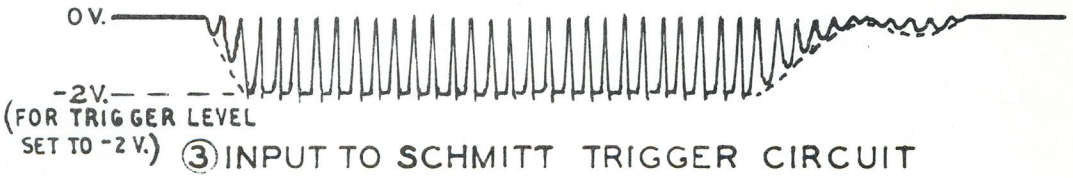
INST. REPORT 25
FIG. 5



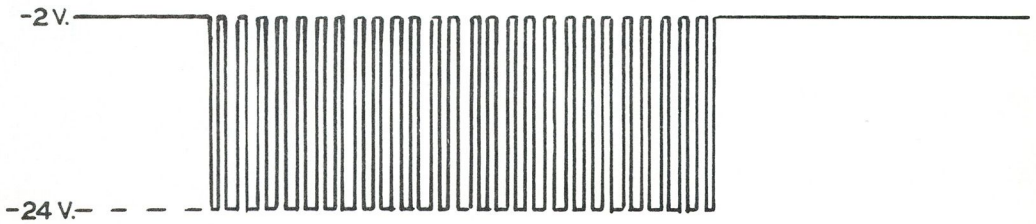
① TYPICAL DECODER INPUT SIGNAL
(13 COMPLETE CYCLES IN RECORDED BURST)



② RECTIFIED WAVEFORM



③ INPUT TO SCHMITT TRIGGER CIRCUIT



④ SCHMITT TRIGGER CIRCUIT OUTPUT
(27 PULSES)

TIME SCALE: 1 INCH ≡ $\frac{1}{700}$ SECOND

WAVEFORMS RELEVANT TO FREQUENCY DOUBLER

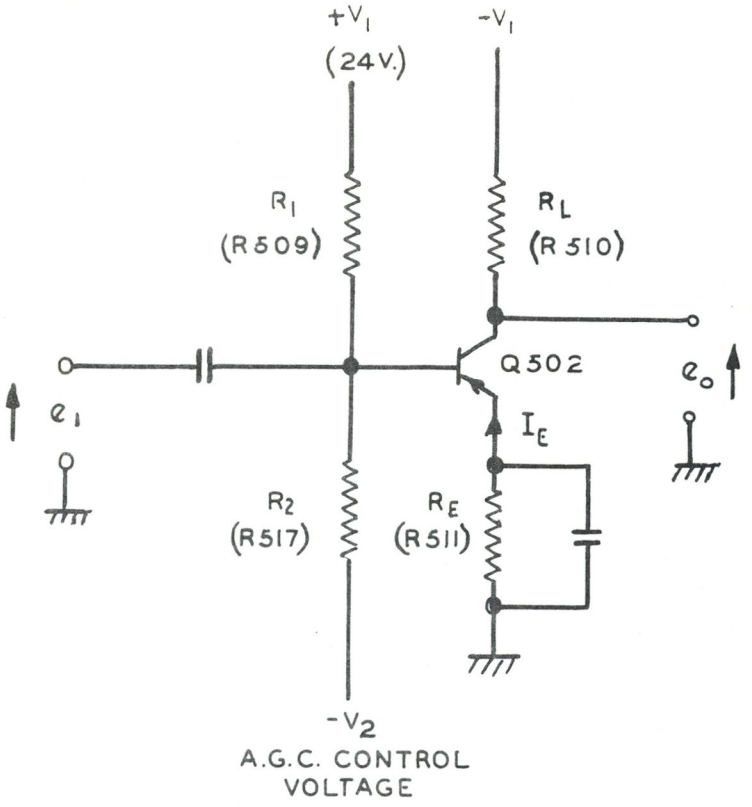


FIG. 7(a) CIRCUIT OF GAIN CONTROLLED AMPLIFIER

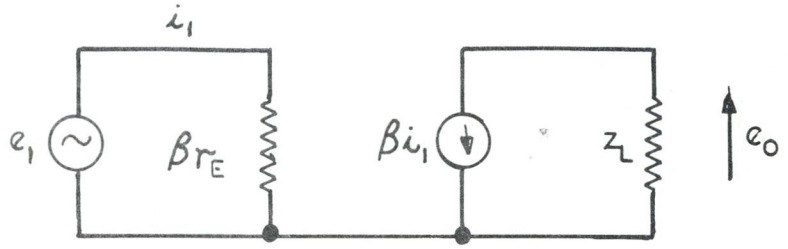


FIG. 7(b) SMALL SIGNAL EQUIVALENT CIRCUIT

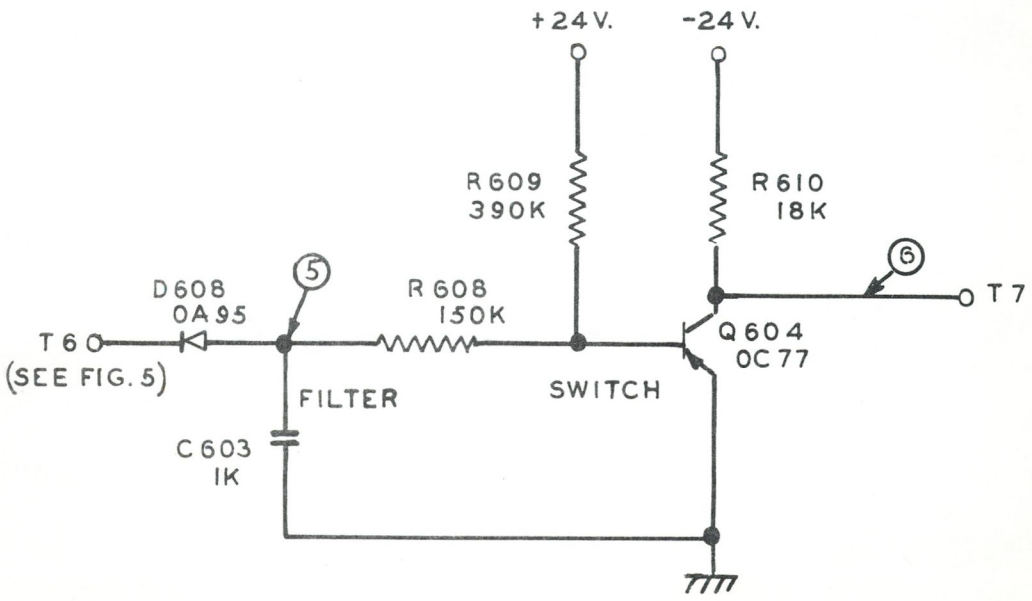
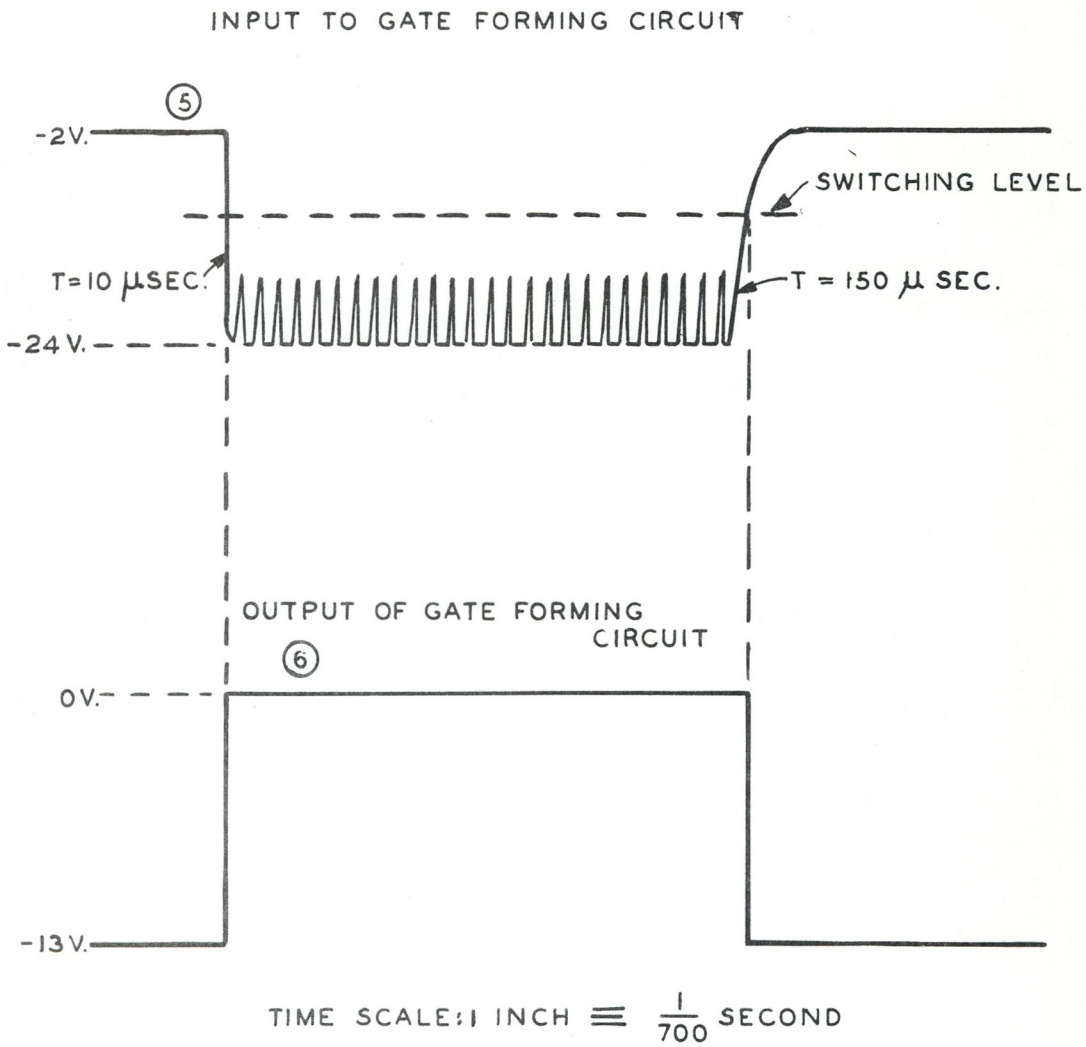
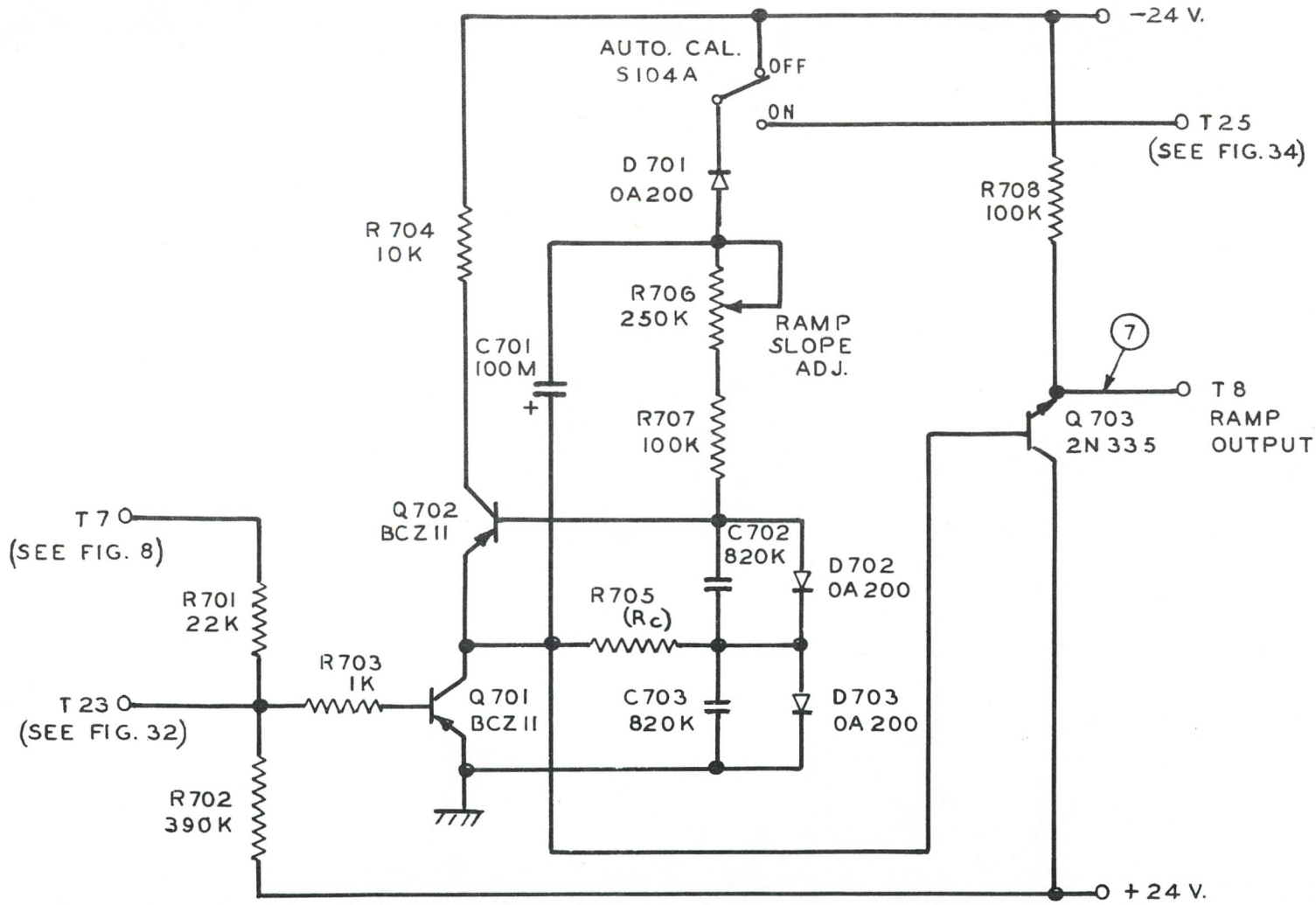


FIG. 8 GATE FORMING CIRCUIT



WAVEFORMS RELEVANT TO GATE FORMING CIRCUIT



RAMP GENERATOR

INST. REPORT 25
FIG.10

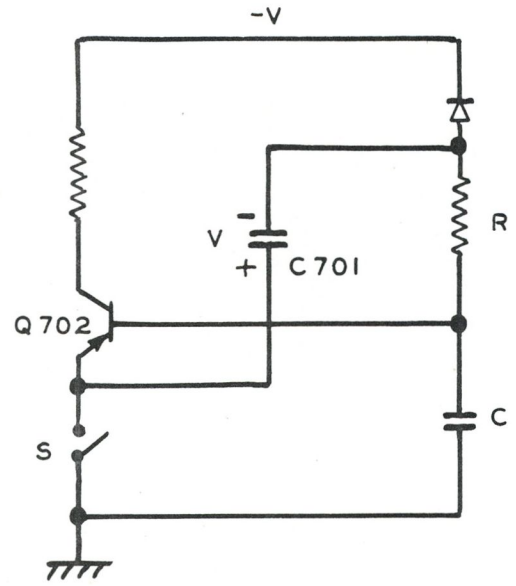


FIG. 11(a) CONVENTIONAL CIRCUIT

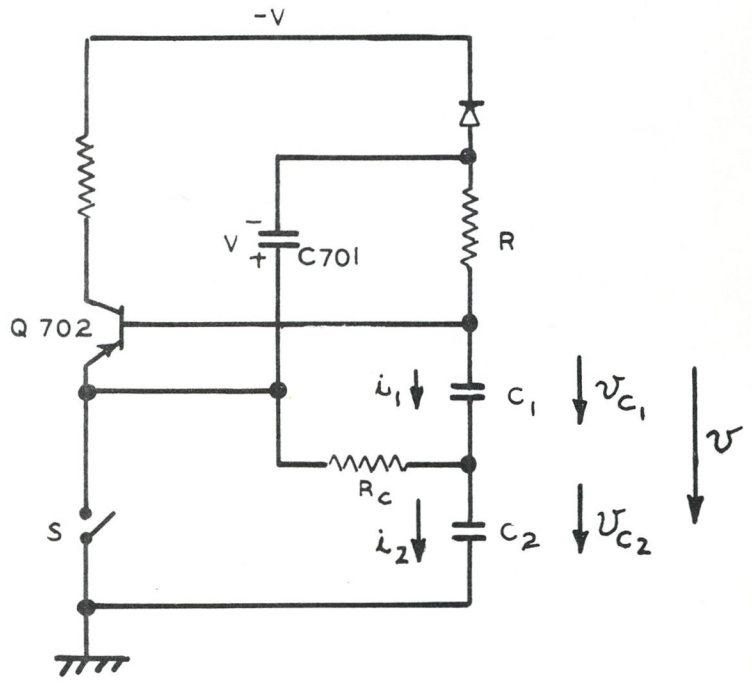
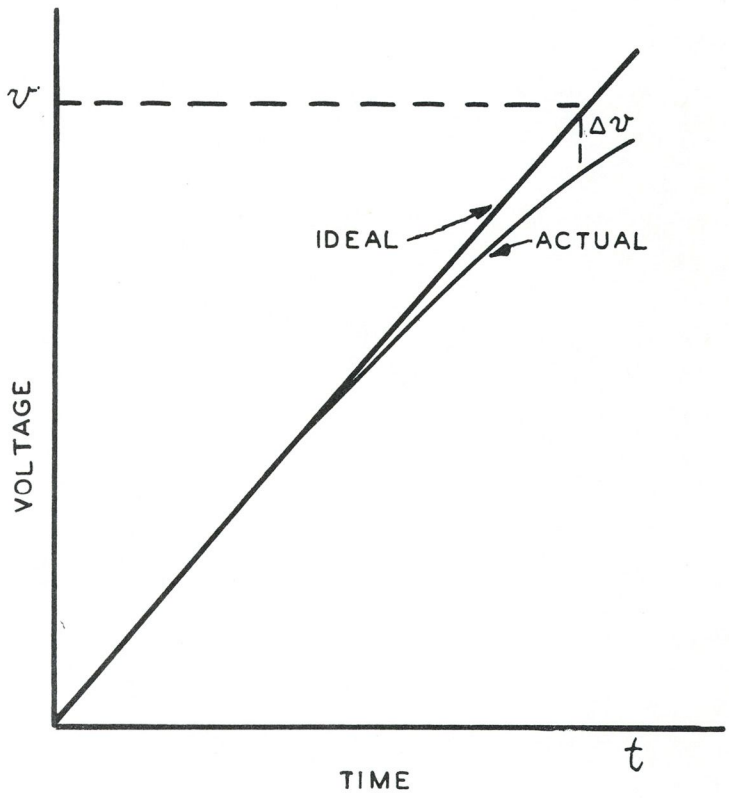
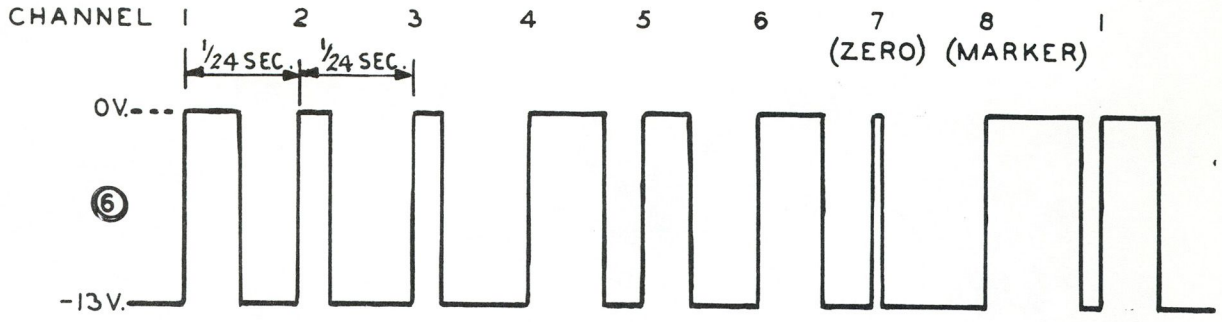


FIG. 11(b) COMPENSATED RAMP CIRCUIT

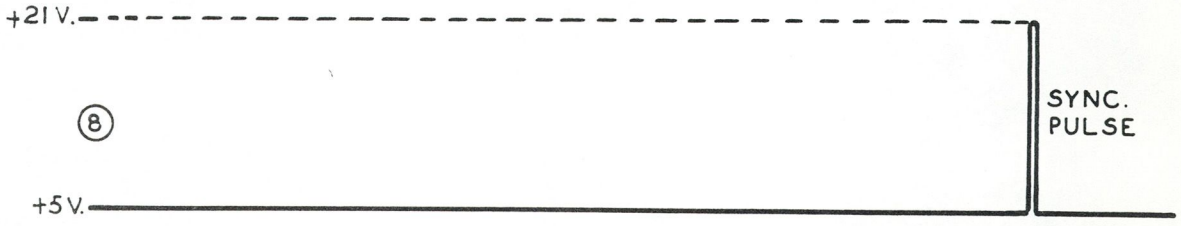


CURVE SHOWING DEPARTURE OF RAMP FROM LINEARITY

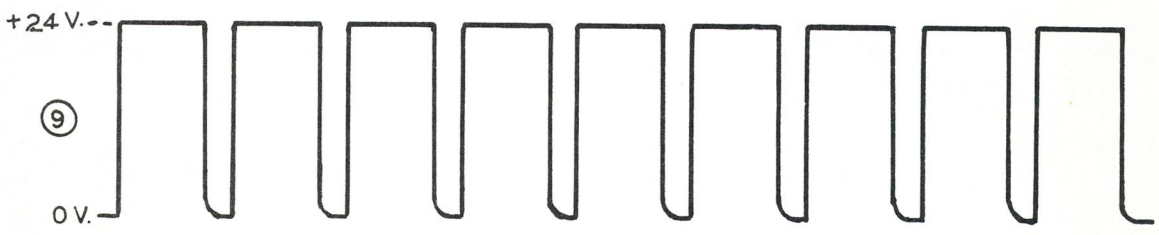


OUTPUT OF GATE FORMING CIRCUIT

RAMP GENERATOR OUTPUT



VOLTAGE COMPARATOR OUTPUT



OSCILLATOR OUTPUT (SYNCHRONISED)

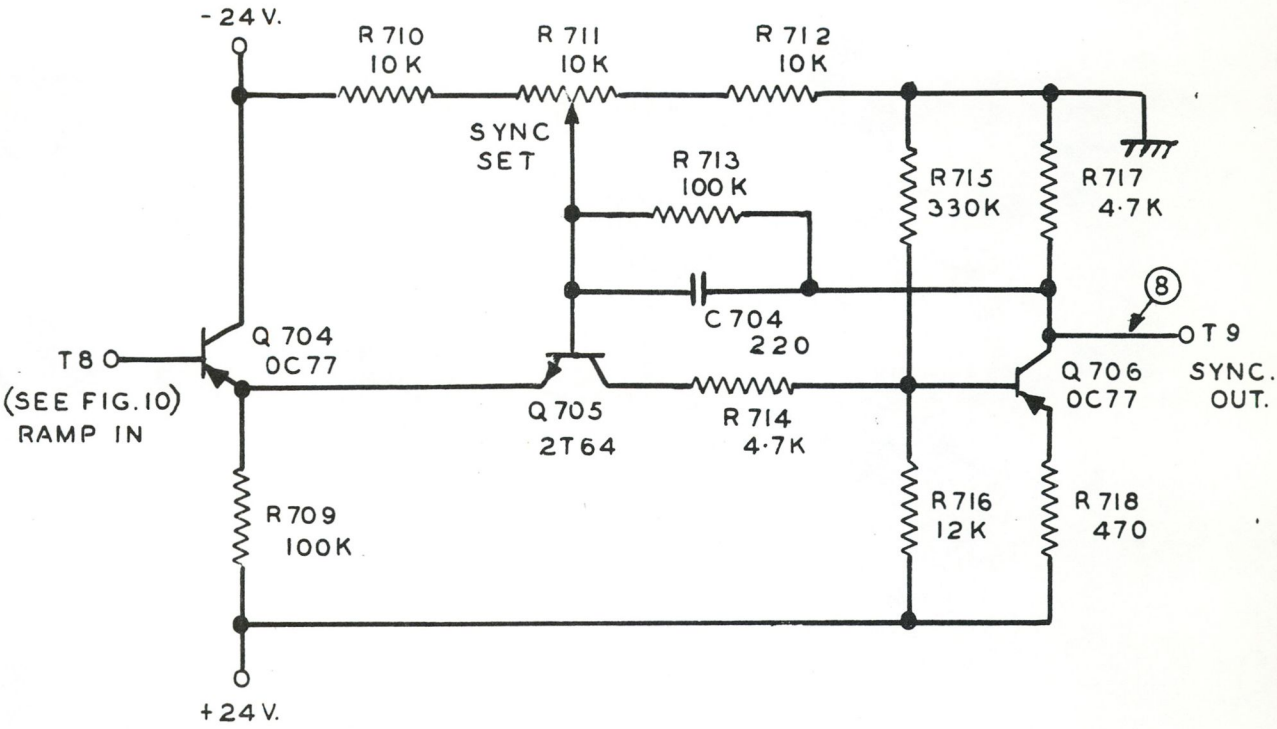


FIG. 14 VOLTAGE COMPARATOR

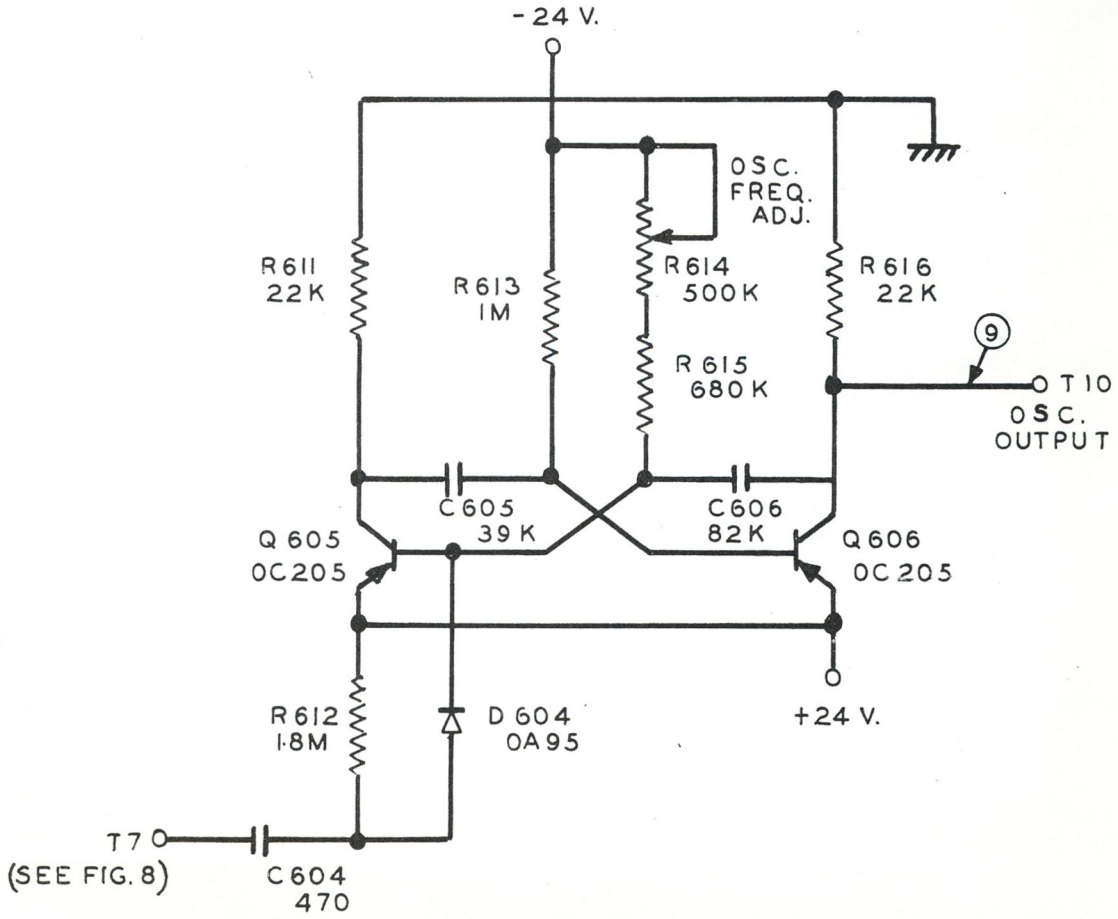
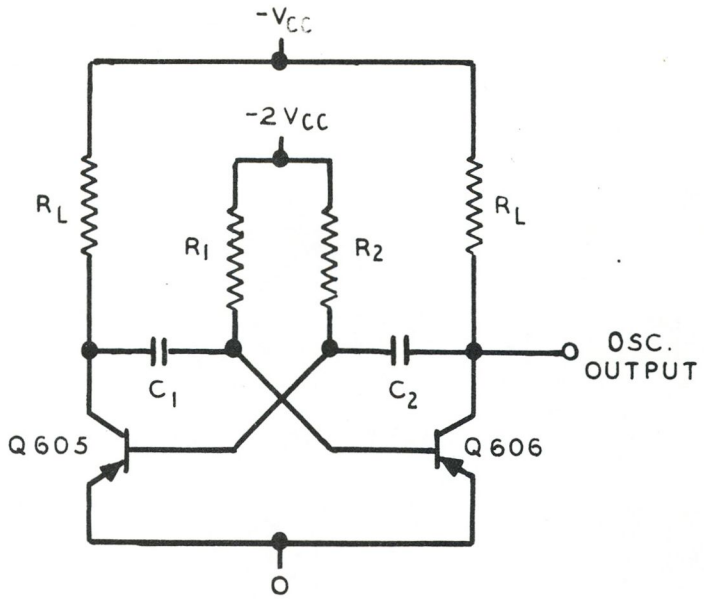
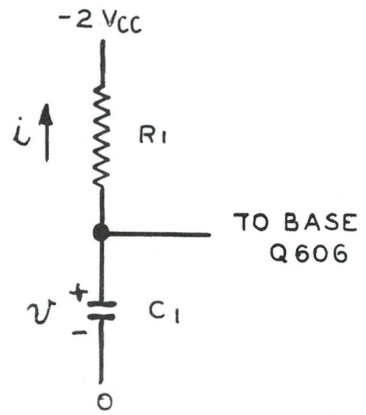


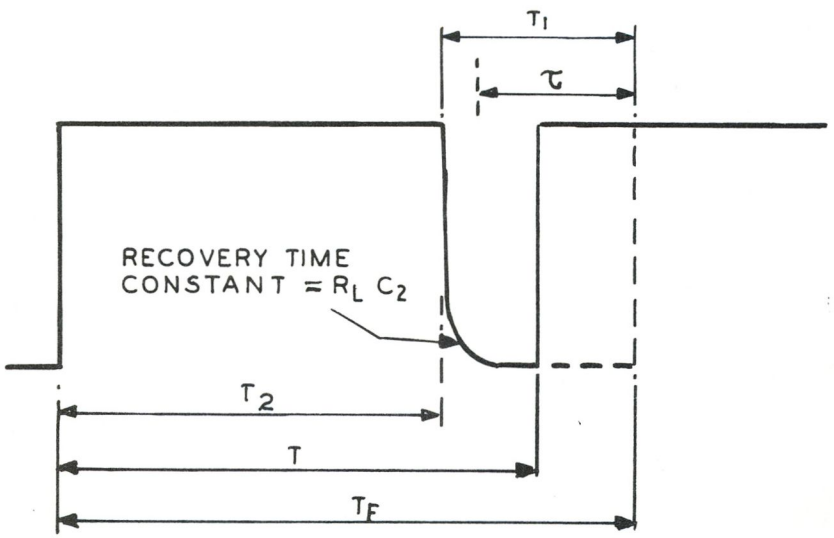
FIG. 15 SYNCHRONISED OSCILLATOR



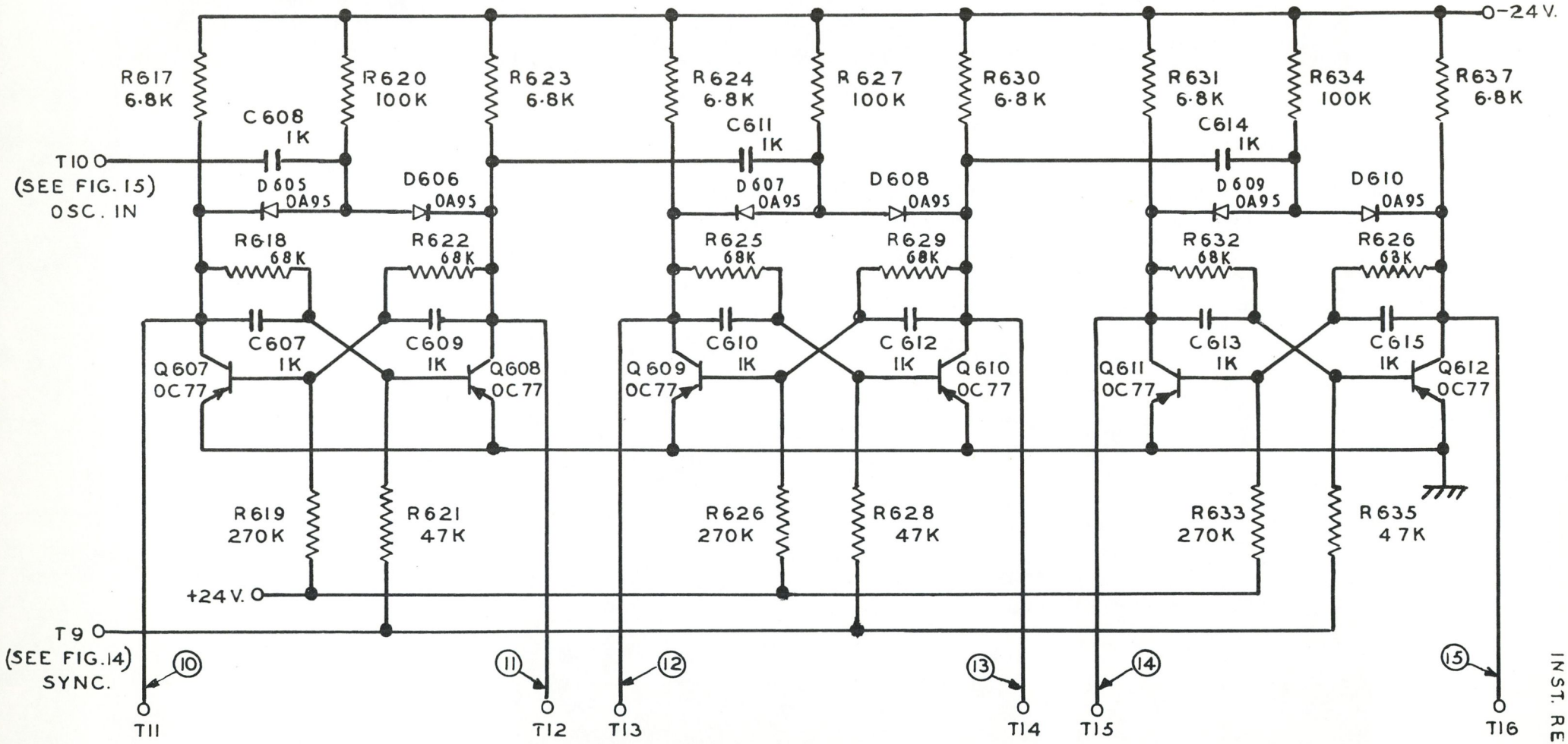
(a) BASIC OSCILLATOR CIRCUIT



(b) EQUIVALENT DISCHARGE CIRCUIT FOR C_1

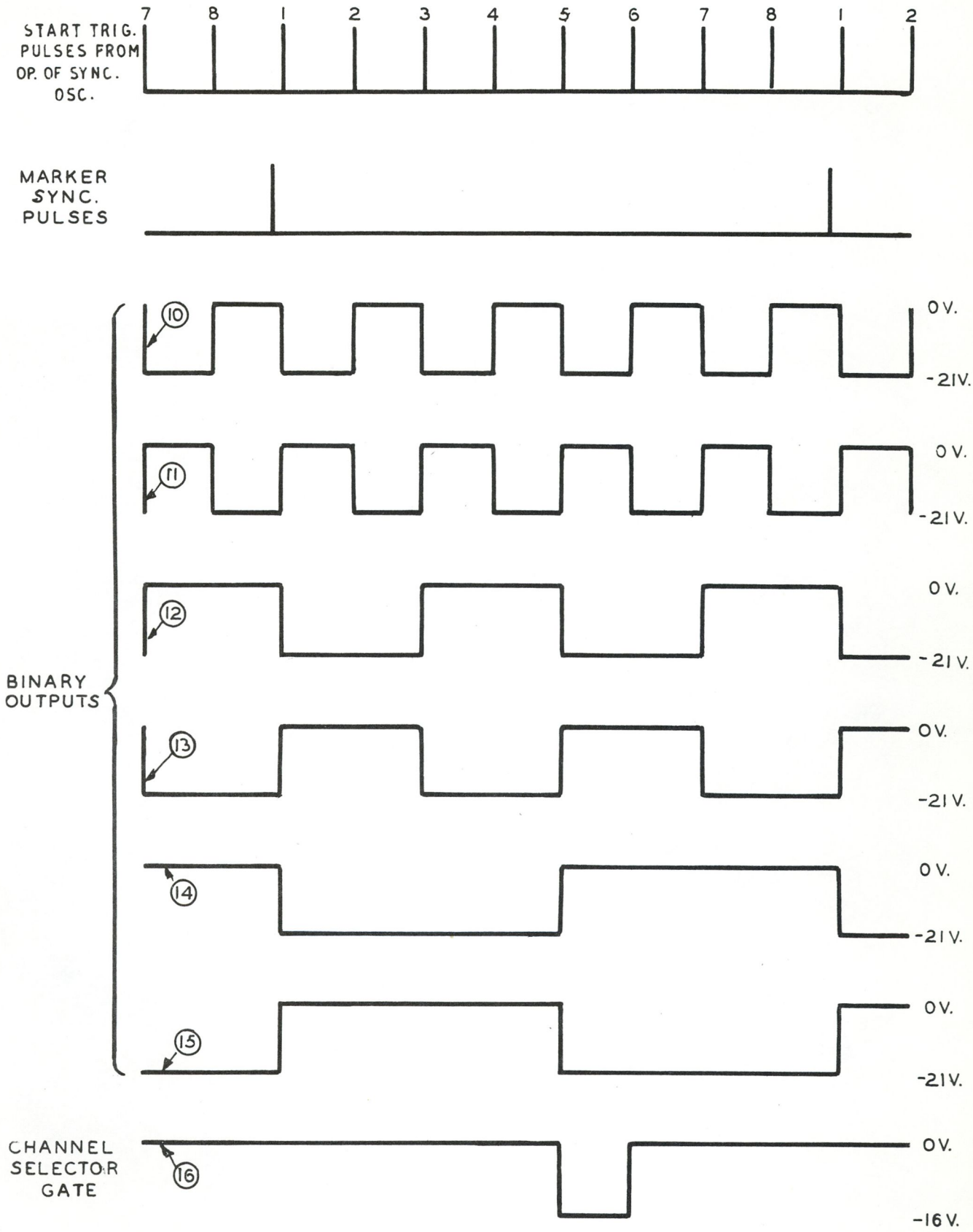


(c) OSCILLATOR OUTPUT WAVEFORM

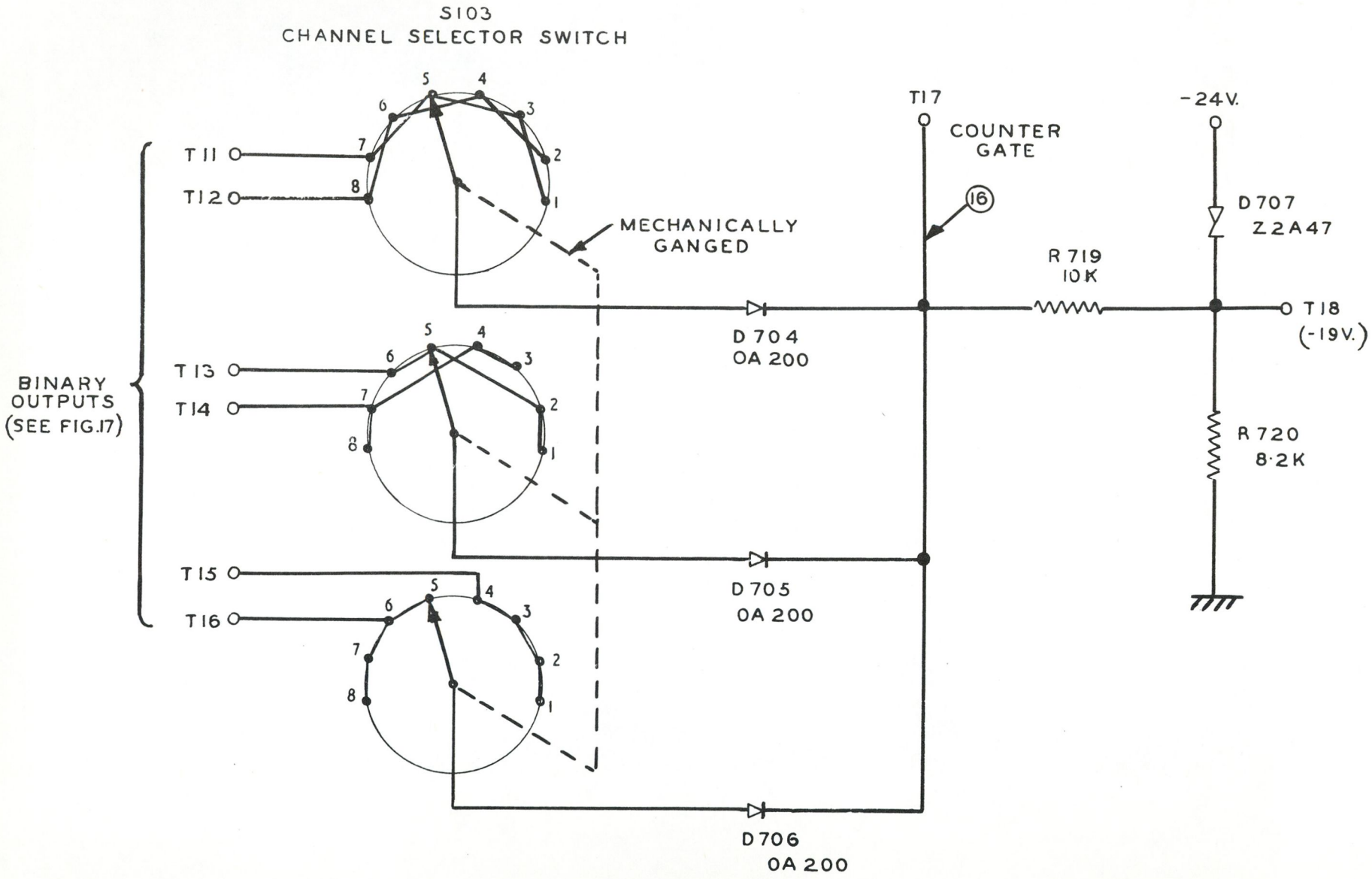


COUNT BY 8 BINARY CHAIN

INST. REPORT 25
FIG. 17

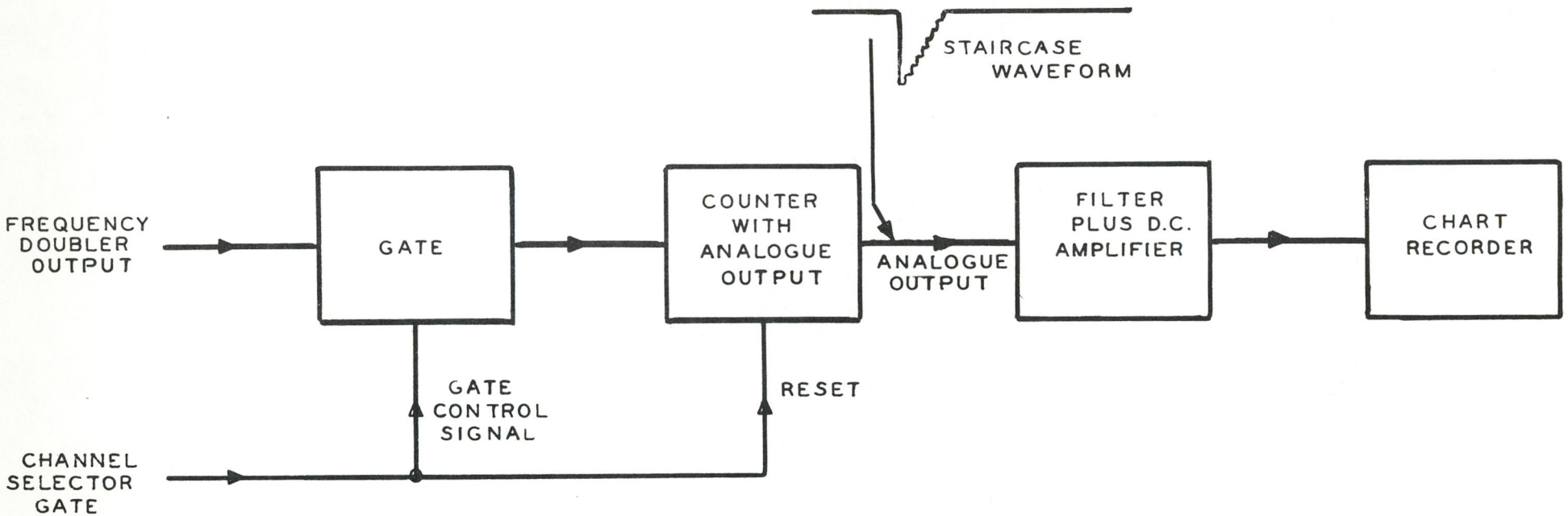


WAVEFORMS RELATING TO BINARY CHAIN & CHANNEL SELECTOR



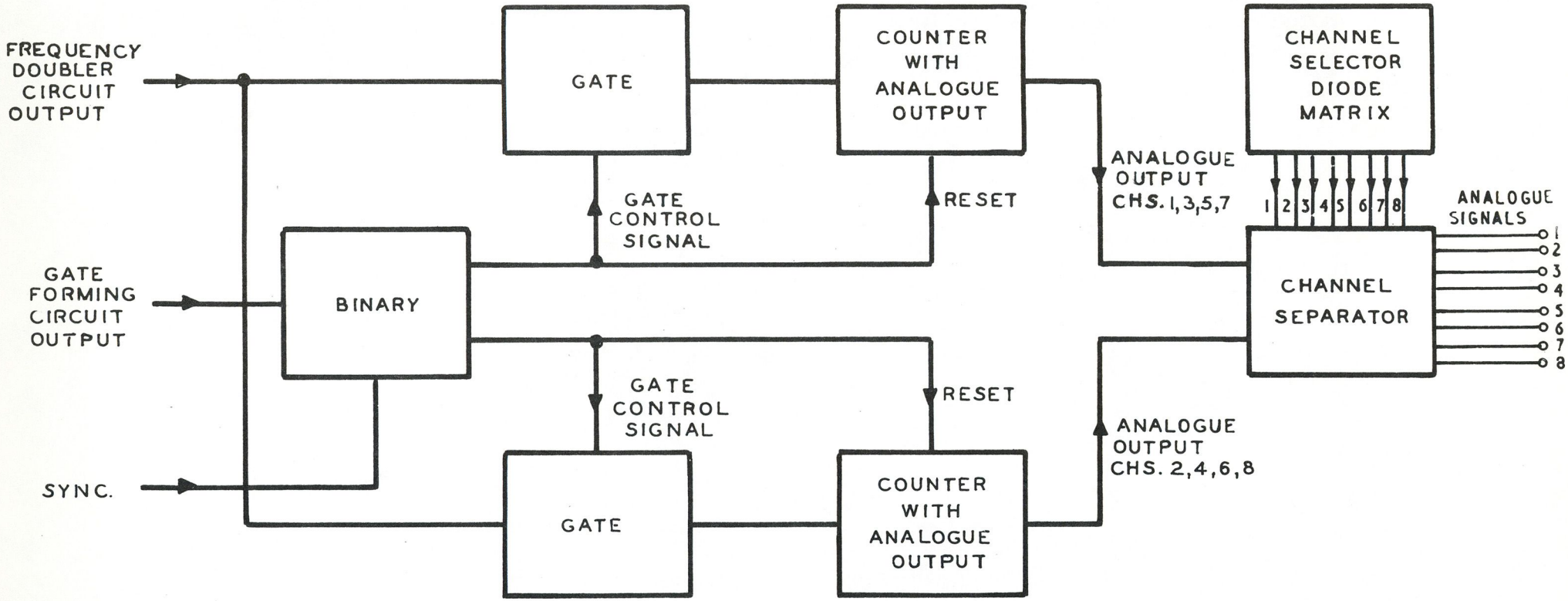
CHANNEL SELECTOR

INST. REPORT 25
FIG. 19



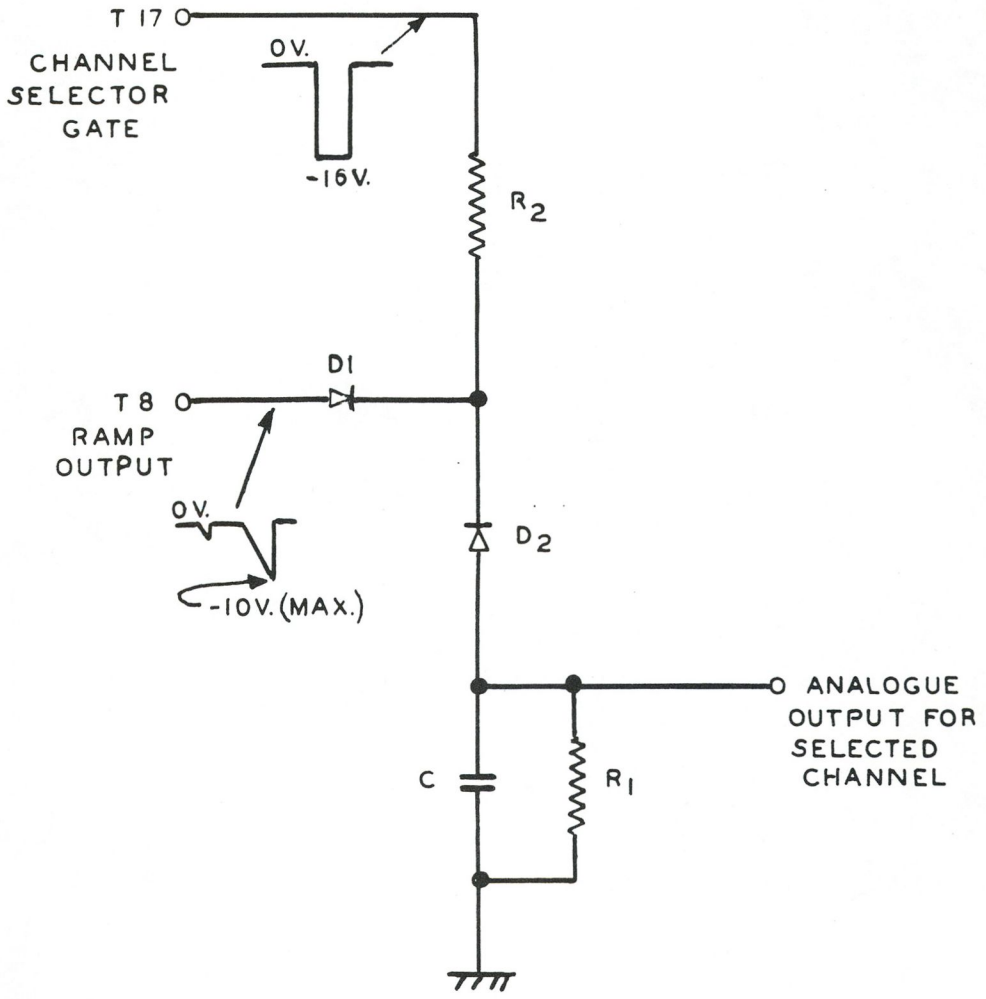
SIMPLE DIGITAL TO ANALOGUE CONVERTER

INST.REPORT 25
FIG.20

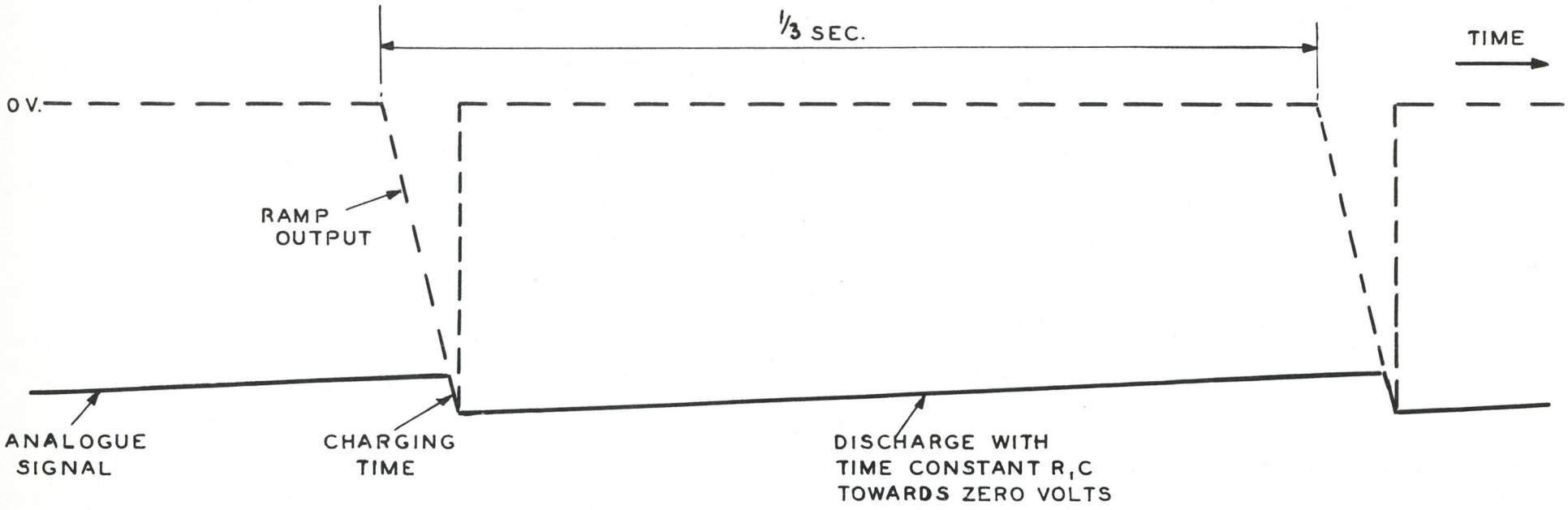


DIGITAL TO ANALOGUE CONVERTER WHICH ENABLES ALL CHANNELS TO BE PRESENTED SIMULTANEOUSLY

INST. REPORT 25
FIG. 21

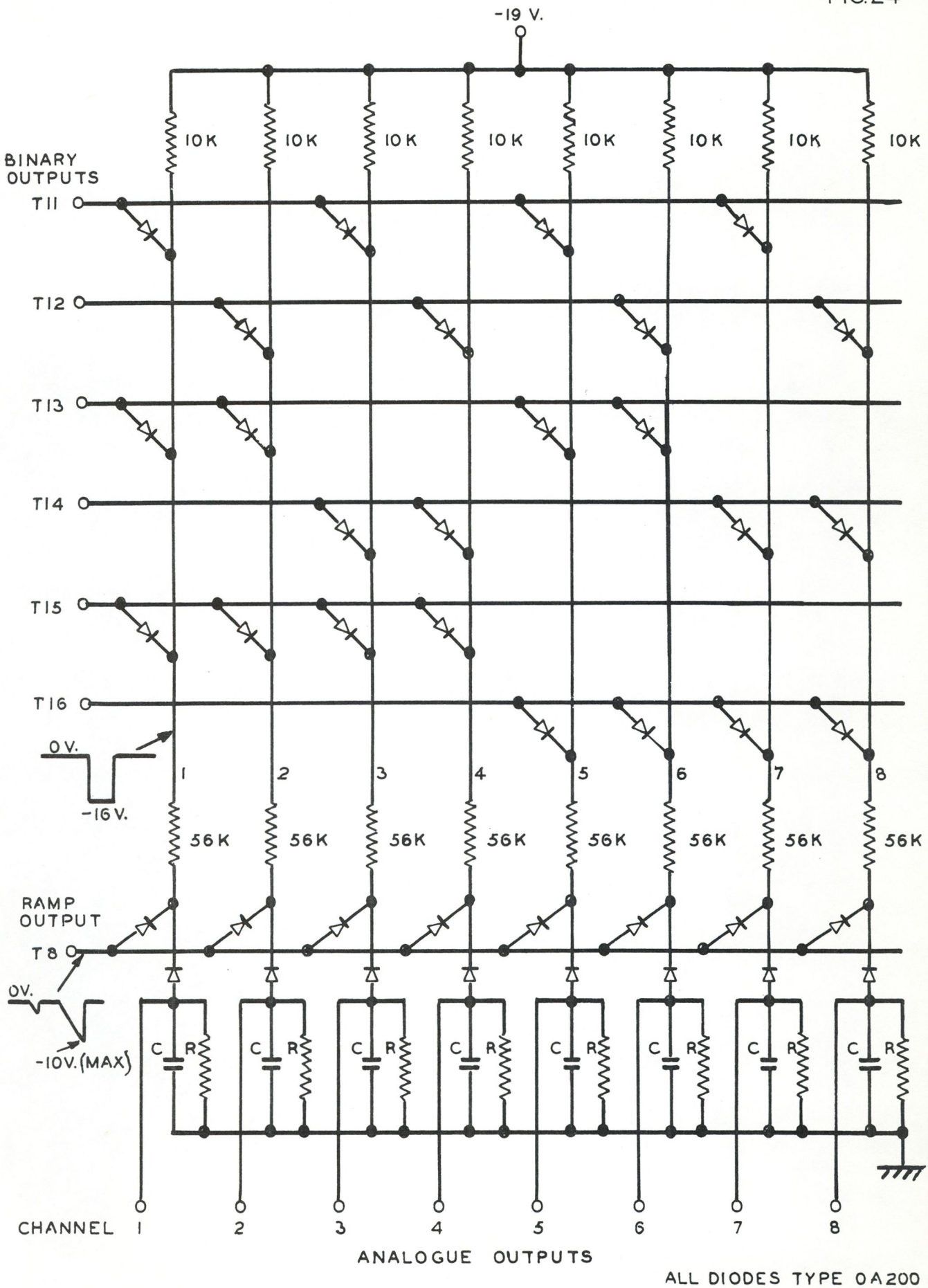


SIMPLE CIRCUIT FOR SINGLE CHANNEL VOLTAGE ANALOGUE



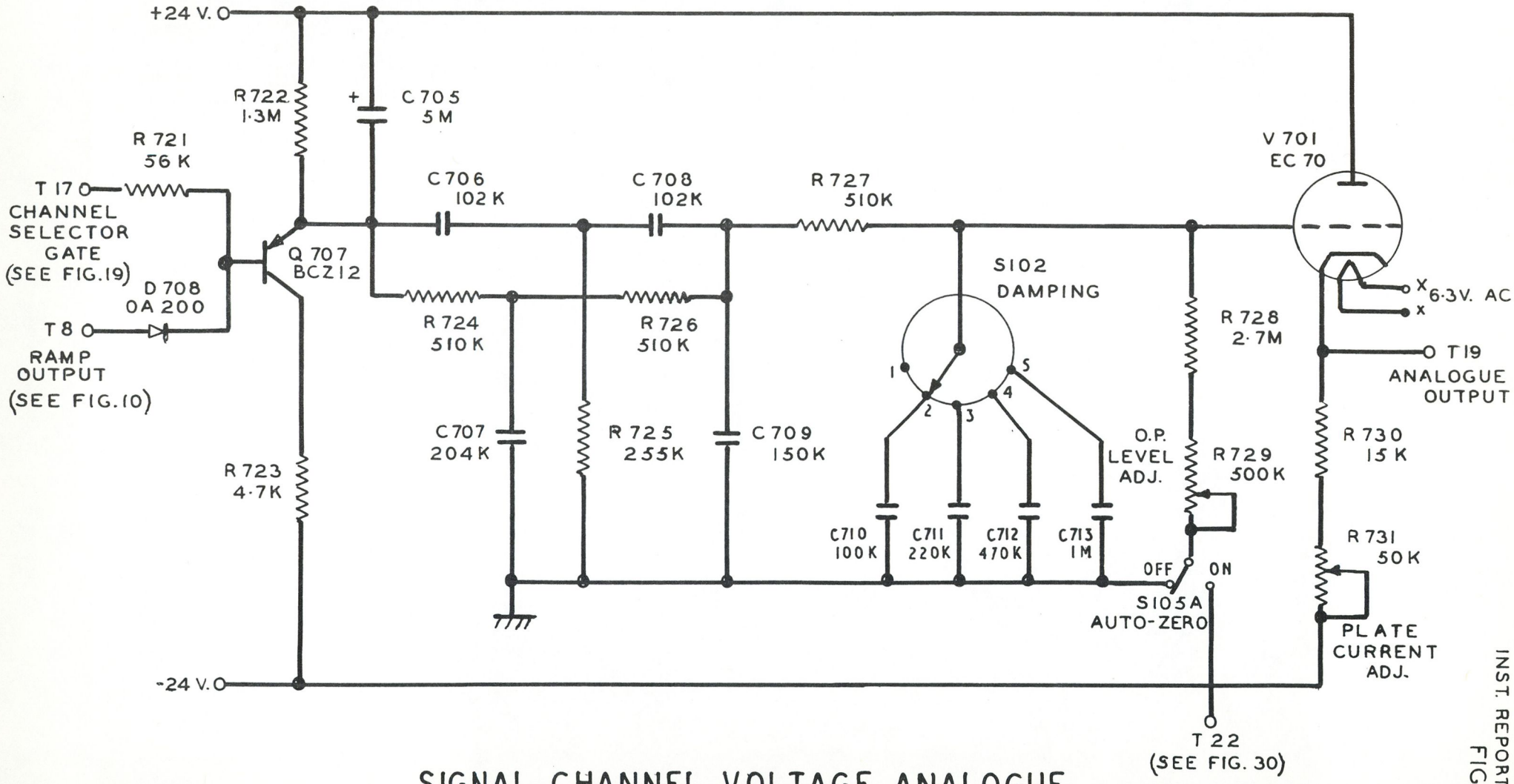
OUTPUT FOR SIMPLE VOLTAGE ANALOGUE CIRCUIT

INST. REPORT 25
FIG. 23



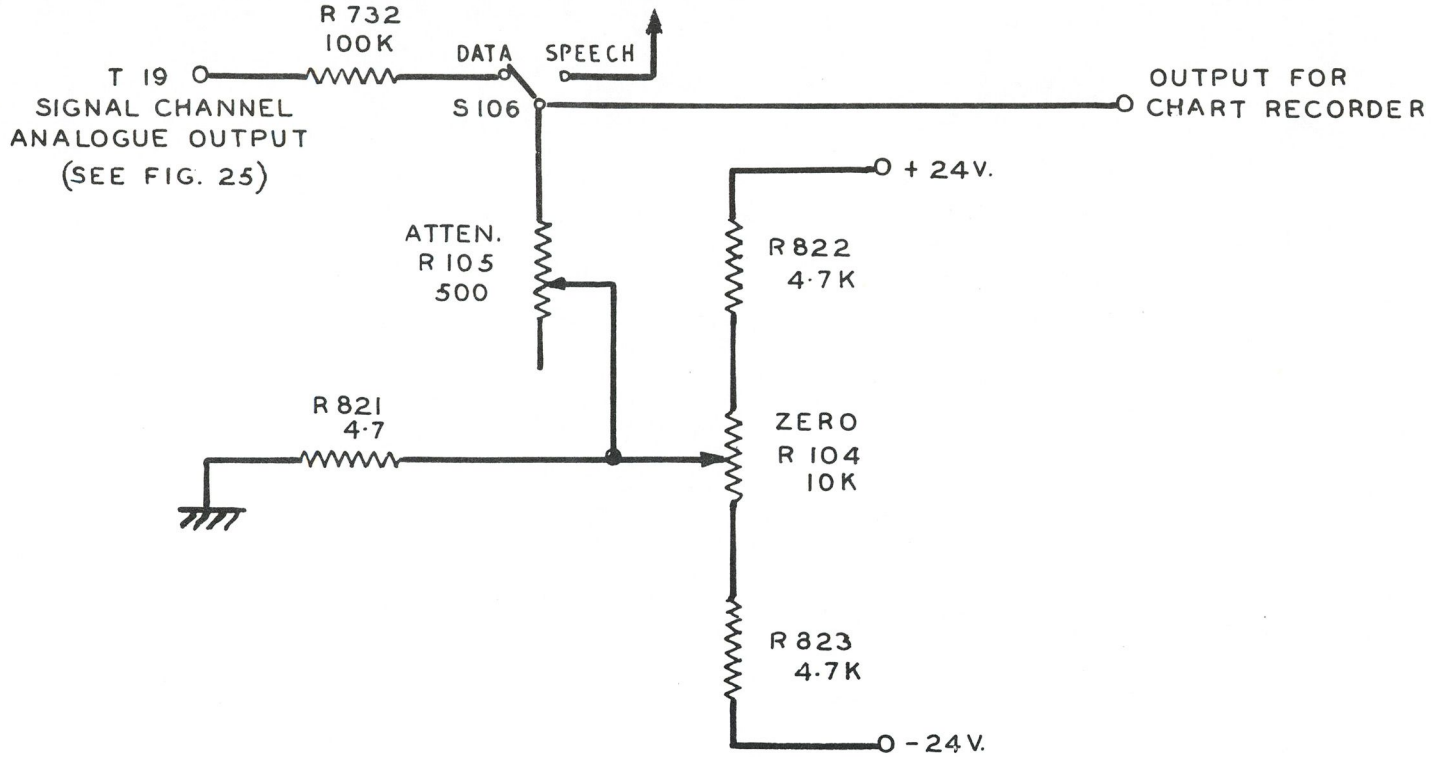
ALL DIODES TYPE OA200

SIMPLE CIRCUIT FOR SIMULTANEOUS VOLTAGE ANALOGUE OF ALL CHANNELS



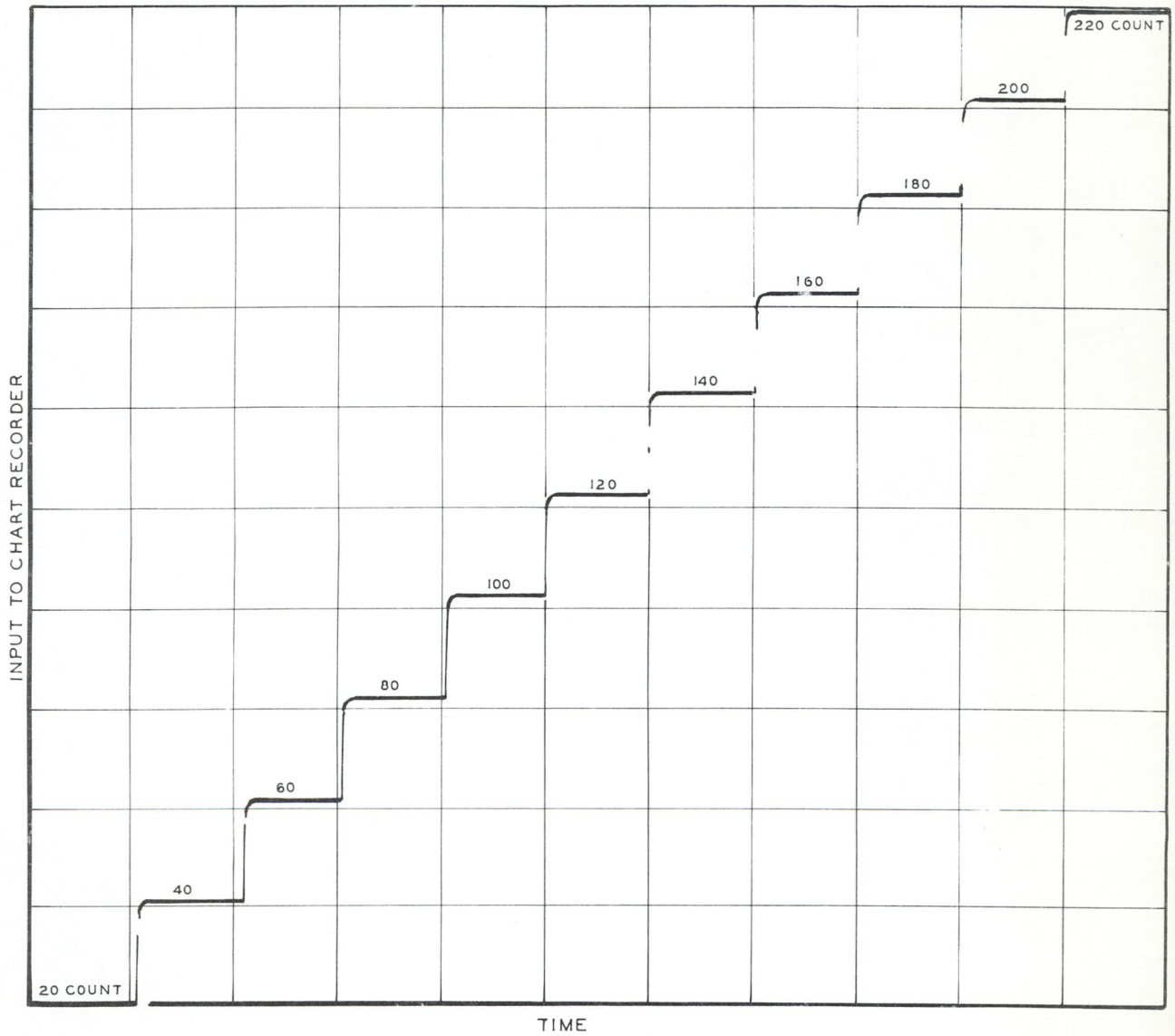
SIGNAL CHANNEL VOLTAGE ANALOGUE

INST. REPORT 25
FIG. 25

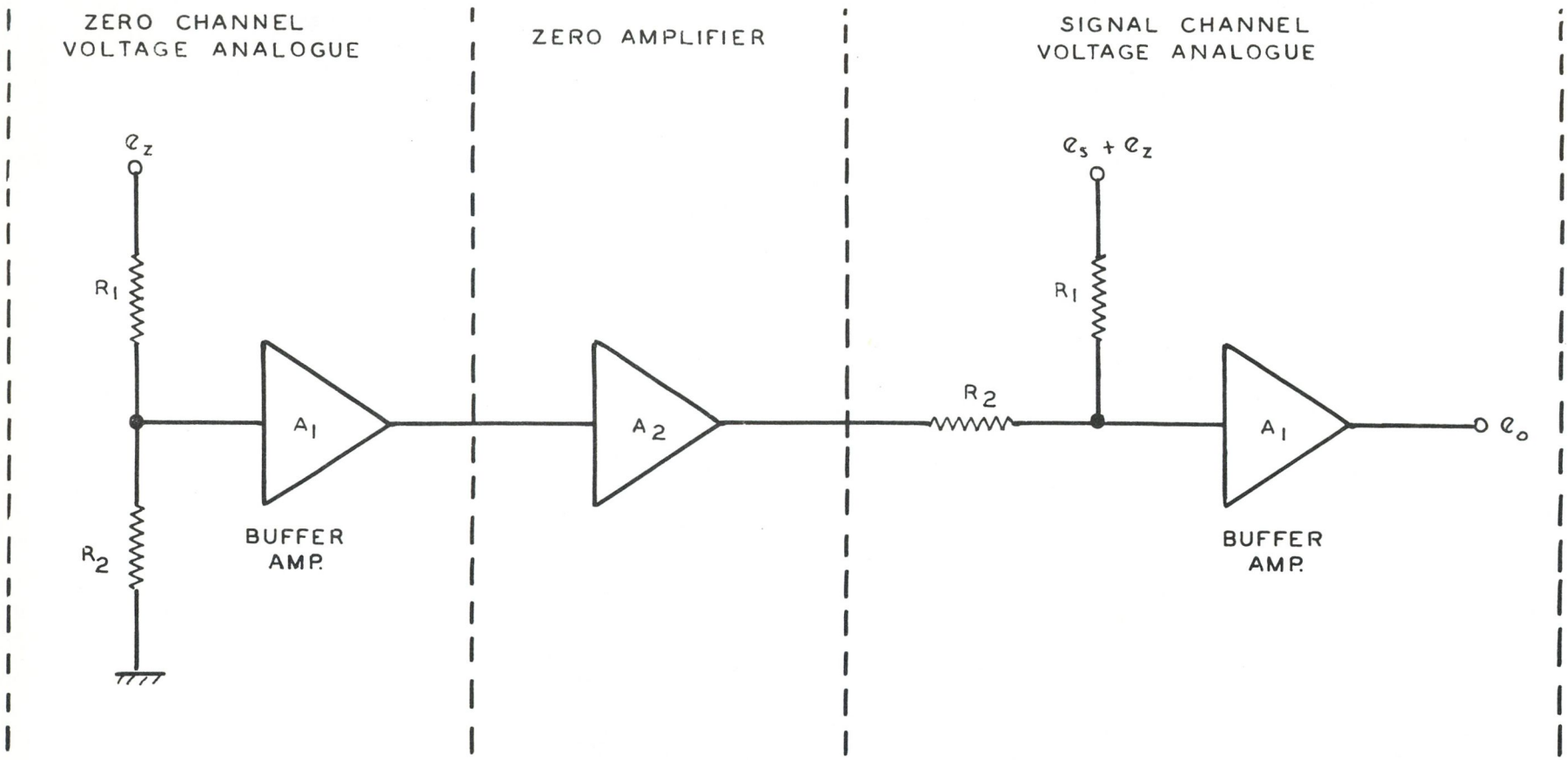


ANANOGUE OUTPUT FOR SPEEDOMAX RECORDER (10mV. FULL SCALE)

INST. REPORT 25
FIG.26

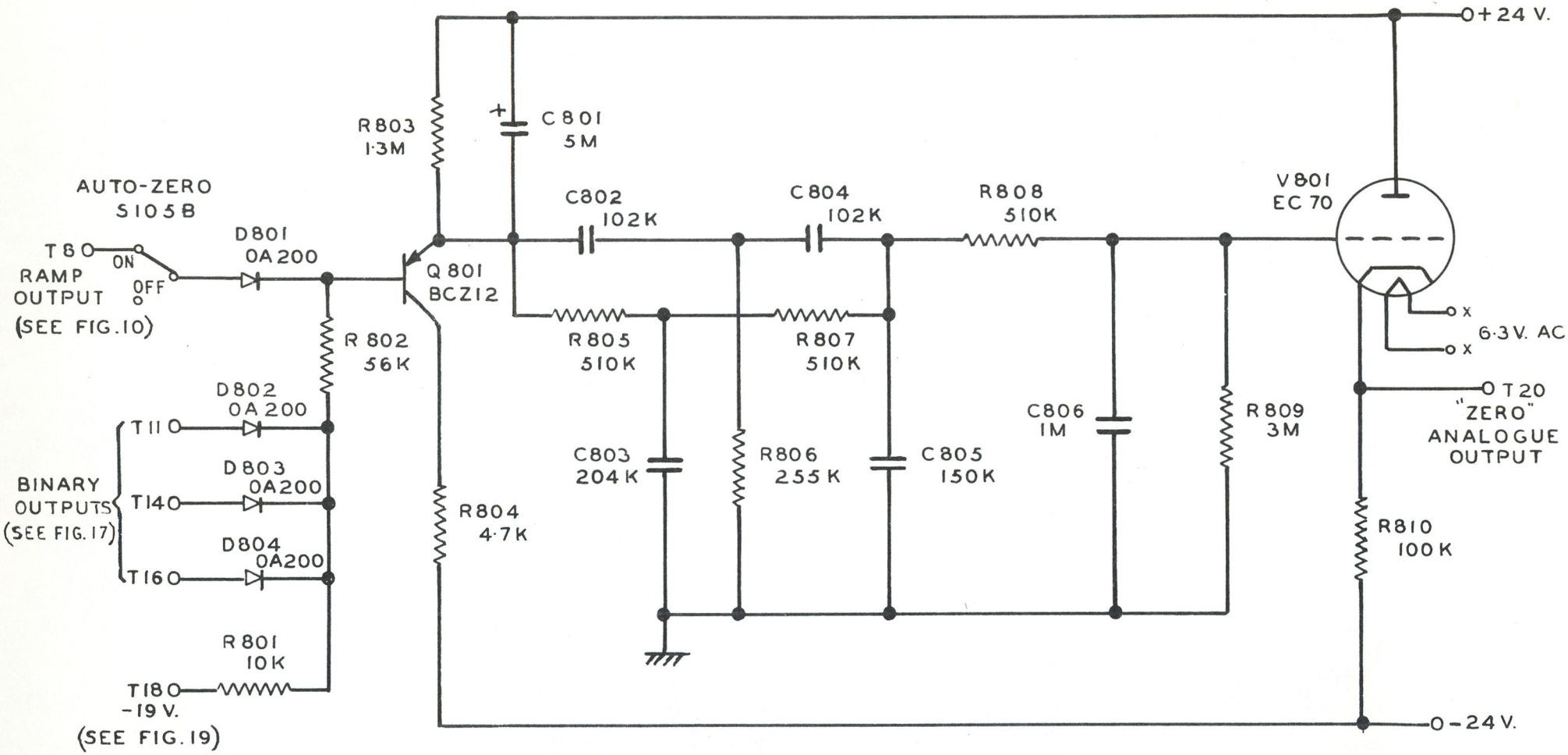


ANALOGUE CIRCUIT LINEARITY



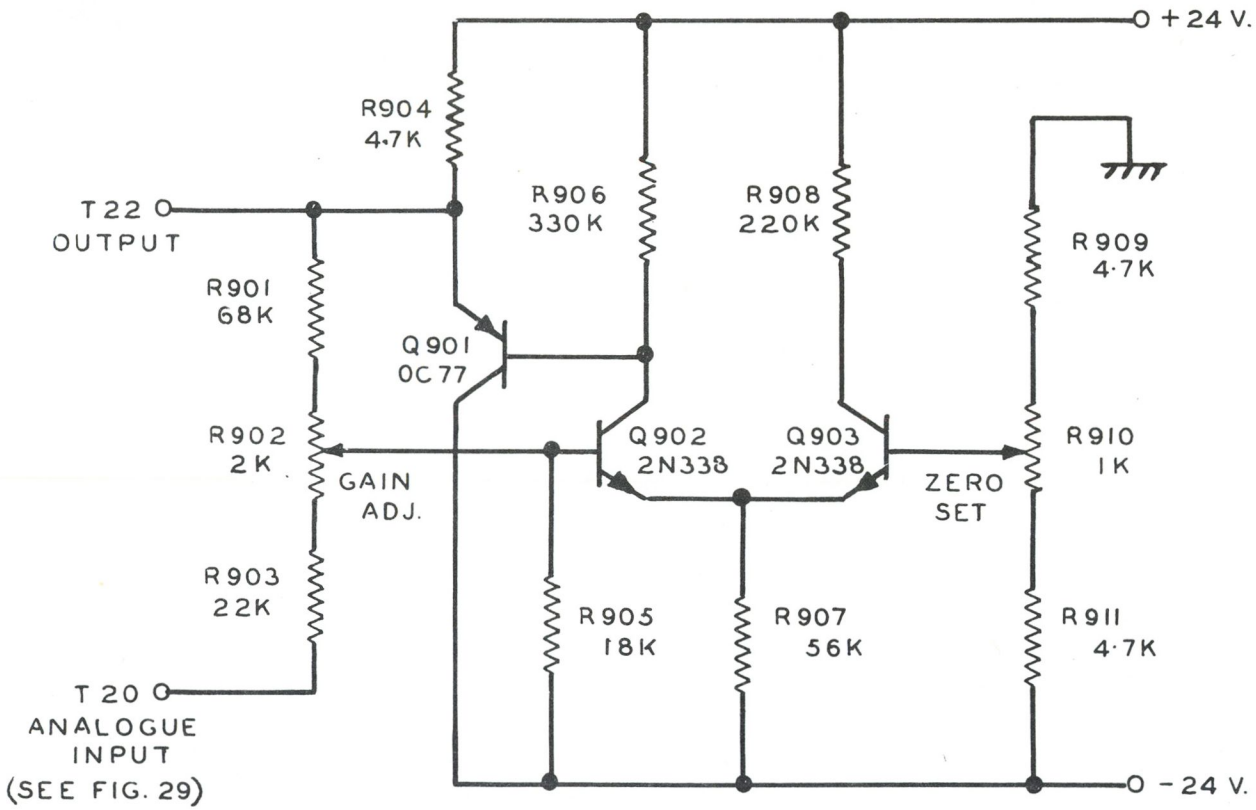
SYSTEM OF AUTOMATIC ZEROING

INST. REPORT 25
FIG. 28



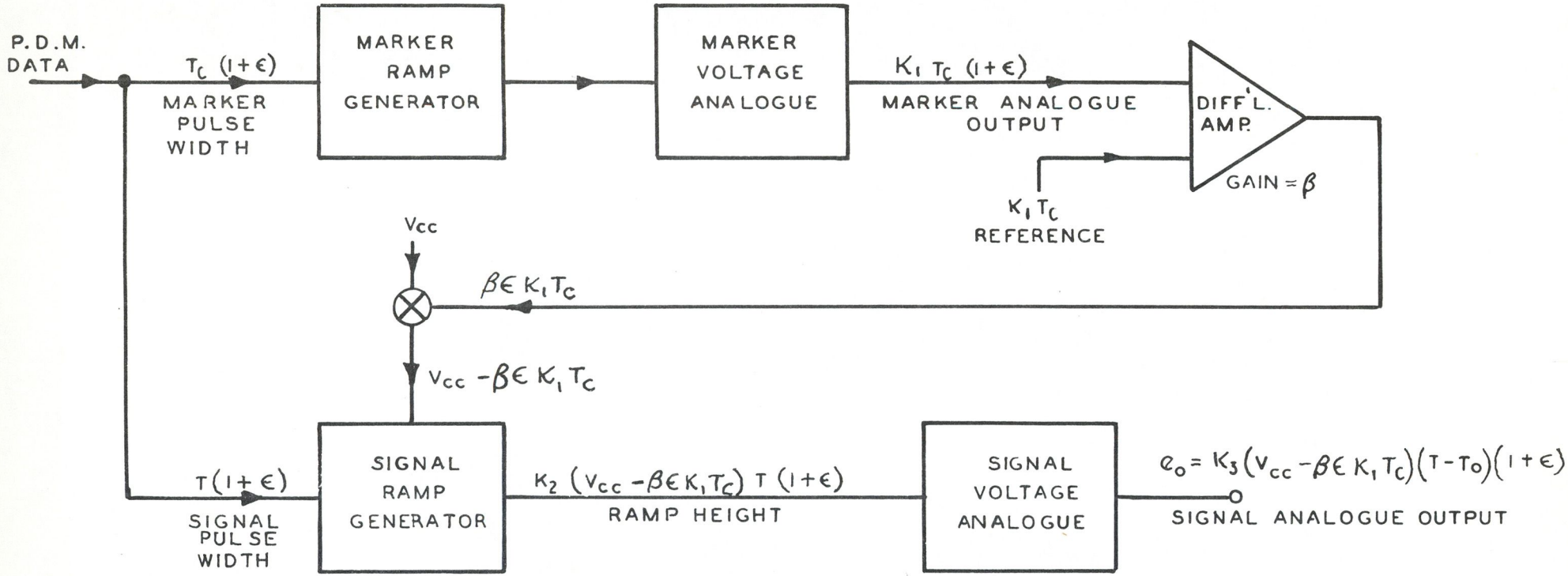
ZERO CHANNEL VOLTAGE ANALOGUE

INST. REPORT 25
FIG.29



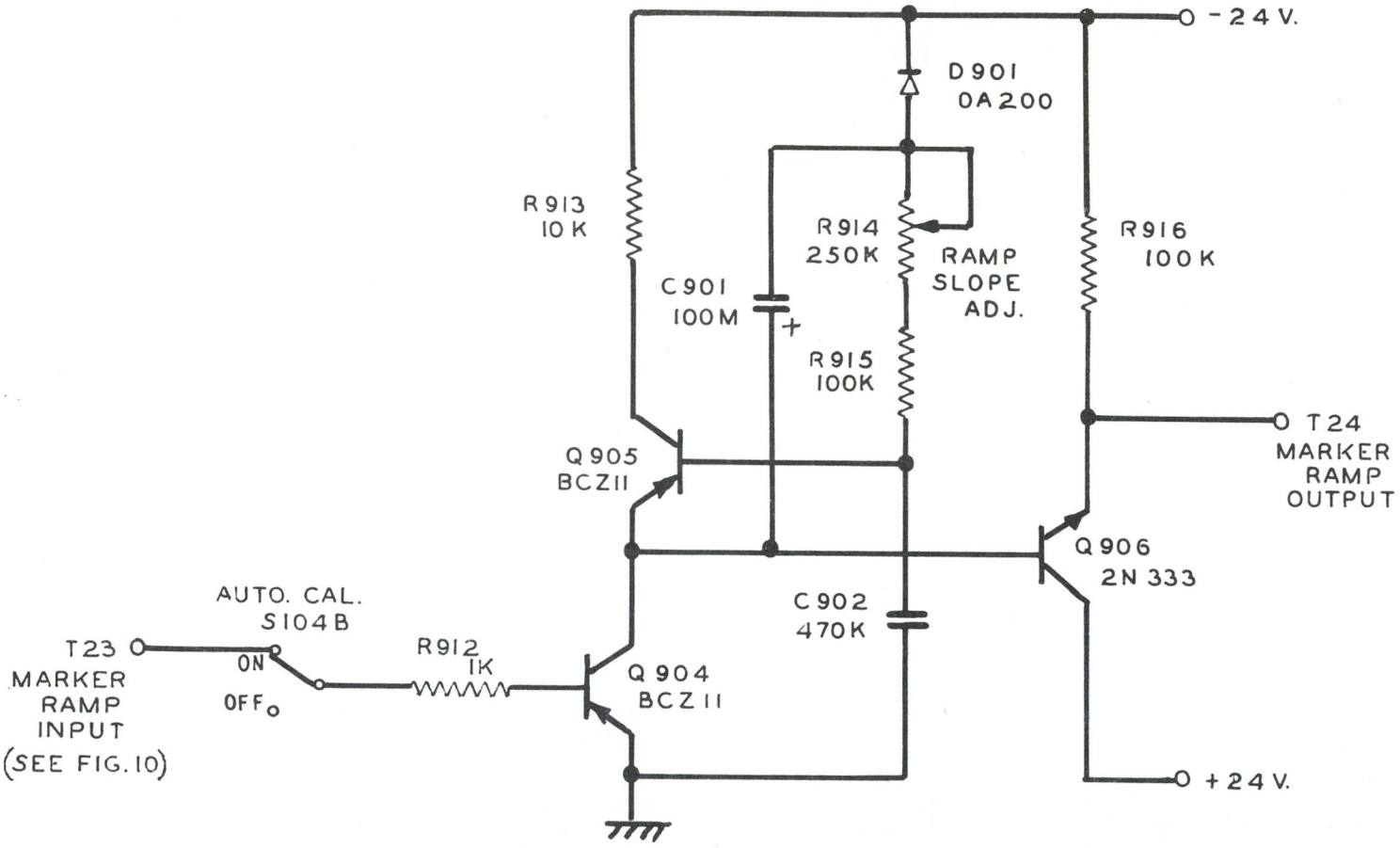
ZERO AMPLIFIER

INST. REPORT 25
FIG. 30



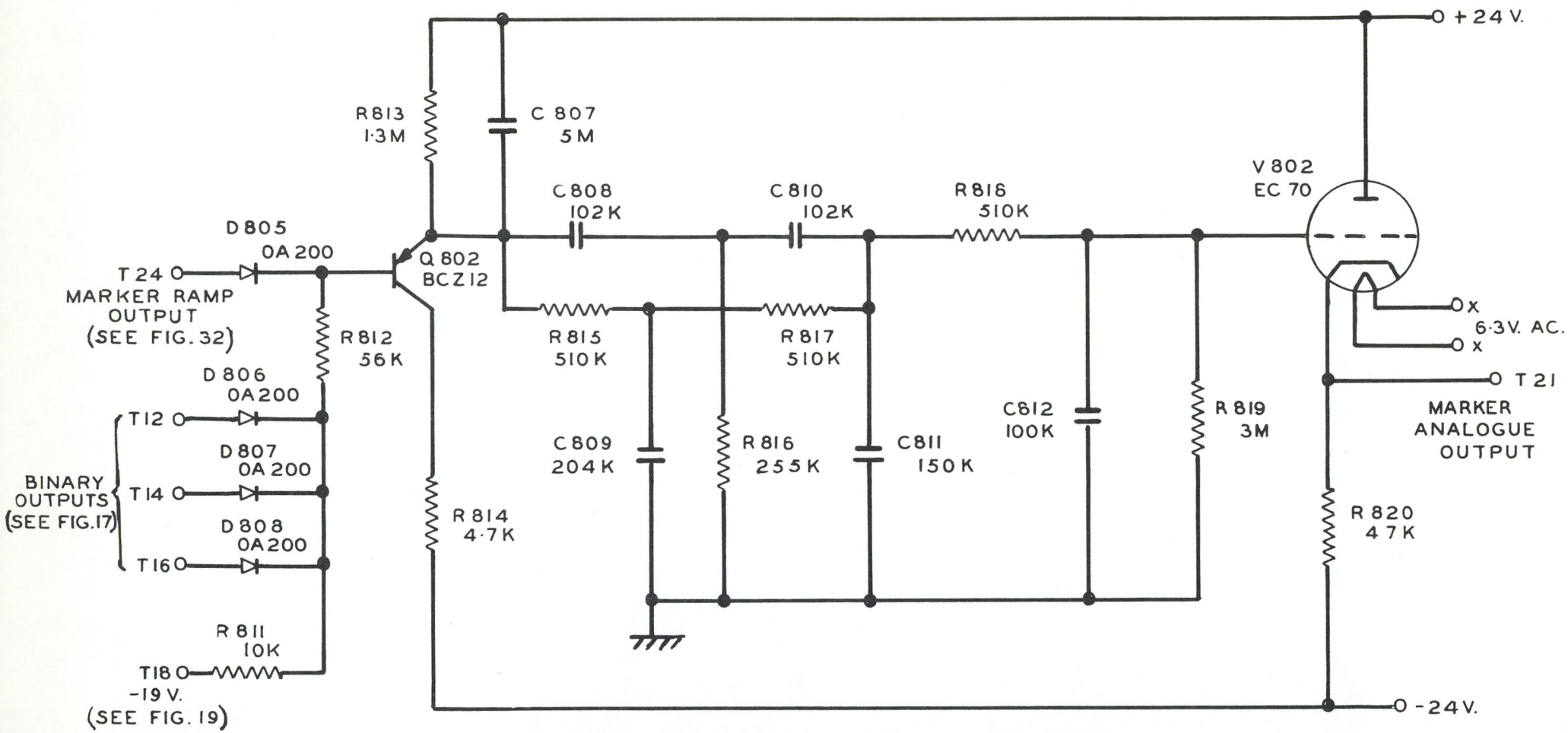
BLOCK SCHEMA OF AUTOMATIC CALIBRATING SYSTEM

INST. REPORT 25
FIG. 31



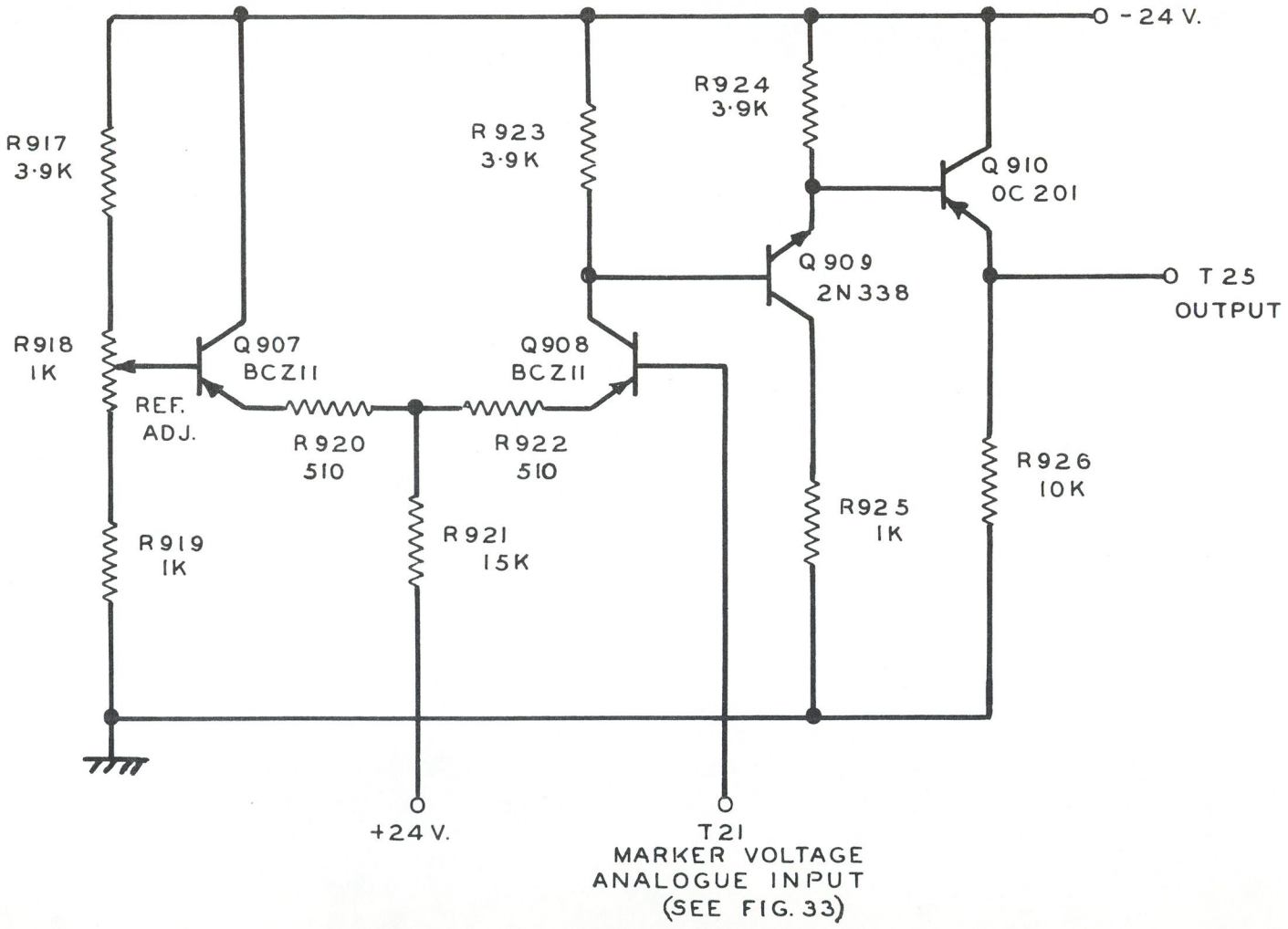
MARKER RAMP GENERATOR

INST. REPORT 25
FIG. 32



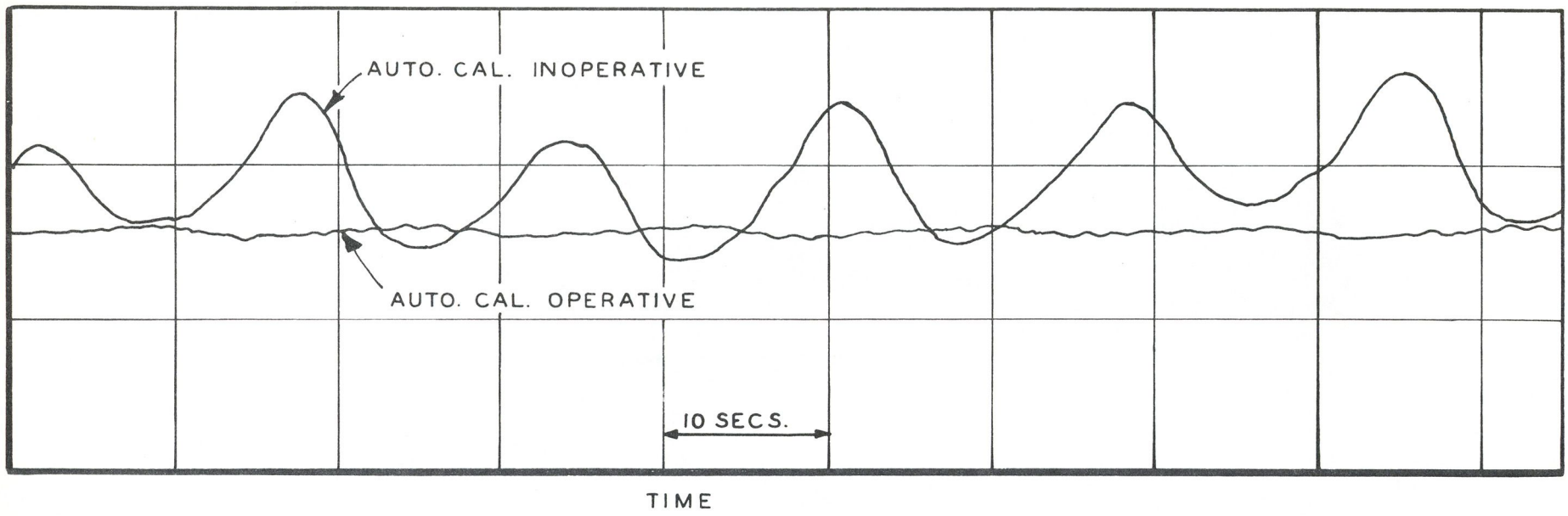
MARKER CHANNEL VOLTAGE ANALOGUE

INST. REPORT 25
FIG. 33



MARKER AMPLIFIER

INST. REPORT 25
FIG. 34



GRAPHS ILLUSTRATING THE ADVANTAGE OF AUTOMATIC CALIBRATION

INST. REPORT 25
FIG. 35