

DEPARTMENT OF SUPPLY
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Instruments Technical Memorandum 51

PULSE FREQUENCY DIVIDER UNIT FOR
USE IN SFIM RECORDER TIMING.

by

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SUMMARY

If the A.R.L. (Aeronautical Research Laboratories) timing system is used in conjunction with the Eclair Type U51 Cine-theodolite for missile tracking purposes the frequency of the timing pulses fed to the Eclair Camematic camera section is too high to be resolved on the SFIM recorder section which records azimuth and elevation angles on a separate photographic recording paper. To provide correlation between the film of the missile motion taken with the Eclair camera and the recording of azimuth and elevation angles taken with the SFIM recorder a common timing source is used. The frequency divider unit, described in this paper, divides the repetition frequency of the pulses from the timing source by 10 and provides an output suitable for driving a SFIM signal detector galvanometer. Under these conditions the timing marks produced on the SFIM recording paper can be readily resolved.

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1. INTRODUCTION

Cinetheodolites are used extensively by A.R.L. (Aeronautical Research Laboratories) for the tracking of moving objects such as missiles and aircraft. Normally these instruments record azimuth and elevation angles on the same frame as the photograph of the moving object. The operation of the Eclair Cinetheodolite Type U51 (used by A.R.L. for tracking purposes) is somewhat different. In this instance the moving object is photographed using an Eclair Model C Camematic camera (a standard 35 mm cine-camera) and the recording of azimuth and elevation angles is made using a separate SFIM Type A22 recorder. In the latter instrument the image of the filament of a recording lamp is reflected by mirrors, comprising the azimuth and elevation measuring elements, on to a moving photographic recording paper thus providing an analogue type of recording.

The present system of providing timing marks on the films taken in missile tracking exercises incorporates a central timing generator which produces pulses at a repetition rate of 25 p.p.s. or 100 p.p.s.. These pulses are amplified by Pulse Amplifier units to a level suitable for flashing neon timing lamps incorporated in the cameras. In the case of the Type U51 Cinetheodolite, timing correlation between the Eclair camera and the SFIM recorder is essential. Timing pulses from a Pulse Amplifier of A.R.L. design are fed to a type NE81 neon which has been incorporated by A.R.L. in the Eclair camera magazine at a position where the film moves continuously. The neon flashes produce timing marks (on the edge of the film) which can be readily resolved at the film frame speed used.

For timing indication purposes the SFIM recorder is fitted with three signal detector galvanometers which deflect beams of light on the recording paper when suitable amplitude signals are applied. The galvanometers are adjusted such that their traces are grouped on the lower edge of the recording paper. One of these galvanometers is connected to a clock escapement timing device in the SFIM recorder which provides 1 second timing marks, another is normally connected to a pair of contacts which close every time the camera shutter opens, and the third is used in the recording of externally applied event marks. The last mentioned galvanometer is the one used for timing indication purposes in missile tracking exercises. At the maximum speed of travel of the recording paper (25 min./sec.) it is not

possible to resolve a timing signal with a repetition rate of 100 p.p.s.. For this reason a pulse frequency divider unit is required to divide the switched timing frequency (25 p.p.s. changing to 100 p.p.s.) by a known integer, say 10, so that individual pulses may be readily resolved on the recording paper. A description of the divider unit used for this purpose follows.

2. GENERAL DESIGN CONSIDERATIONS

As the divider unit is to operate in situations where mains power is not normally available, a self contained power supply is essential. A rechargeable battery pack consisting of 22 Type D4.5 cells of Deac manufacture is used. This battery pack provides a nominal supply voltage of about 29 volt.

Impedance isolation between the divider unit and the source of the incoming timing pulses is a requirement. Hence transformers coupling at the divider input is used.

The divider is housed in a separate box which contains

- (i) A rechargeable battery pack.
- (ii) The divider electronics in the form of a plug-in printed circuit card.
- (iii) A relay circuit to enable remote switching of the divider unit.
- (iv) Test circuits to check for the presence of incoming and outgoing pulses of appropriate amplitude.

The block schematic of Fig. 1 illustrates the relation of the divider unit to other equipment used in the tracking system which incorporates the Eclair Cinetheodolite. Timing pulse generation and remote switching are performed by the Timing Generator. The Eclair Battery Box supplies power for driving the Eclair Cinetheodolite motors and also incorporates a Pulse Amplifier which amplifies the incoming pulses sufficiently to provide an output to flash the camera timing neon. The Frequency Divider Box accepts the pulse input which flashes the camera neon, divides the repetition rate by 10, and provides an output suitable for driving a SFIM galvanometer.

Interwiring within the Divider Box is illustrated in Fig. 2. When power from the Eclair Battery Box is switched onto terminals A and B of the input plug a relay is operated which switches power onto the divider unit.

Complete circuit details of the frequency divider unit are given in Fig. 3.

3. INPUT CIRCUIT

The input to the divider is a high voltage pulse train which is also required to flash the NE81 timing neon in the Eclair Camematic film magazine. Characteristics of the input pulse are summarized below:

Pulse Source Output Impedance:	15,000 ohm.
Pulse Duration	: 0.6 msec nominal (tolerance 0.5 to 1.0 msec)
Pulse Repetition Frequency	: 25 p.p.s. changing to 100 p.p.s.
Pulse Amplitude	: Negative going pulse of approximately 190 volt leading edge dropping rapidly to approximately 80 volt when the neon fires. (If the neon is removed the pulse reaches an amplitude of approximately 250 volt).

To suitably attenuate the input pulse amplitude and at the same time provide isolation between the source of incoming pulses and the pulse divider unit a 10:1 stepdown transformer T1 (See Fig. 3) is used. Series resistor R1 ensures that the divider unit will not, under any circumstances, load the pulse source sufficiently to cause the neon to flash unreliably. To suppress the reverse polarity pulse which causes "double pulsing" of the neon, the diode D1 is placed across the transformer primary.

The shape of the pulse to the neon is virtually unaffected by the connection to the frequency divider unit. The only noticeable effect is a decrease in the recovery time (the time for the pulse to decay to zero on the trailing edge of the pulse as the neon extinguishes).

Initially the pulse (of approximately 9 volt leading edge amplitude) appearing on the secondary of T1 was used to trigger directly the following binary divider chain. As the waveform appearing on the secondary of T1 is not particularly smooth (actually slope

reversal occurs on part duration through the pulse) it was possible under these conditions to divide by 5 instead of by 10. Capacitive loading of the input line tended to accentuate the "double" trigger effect. To eliminate this problem the present circuit first integrates the secondary pulse using the R₂ - C₁ combination and then amplifies the integrated pulse with Q₁ to obtain a sharp pulse suitable for triggering the binaries. Silicon diodes D₂ to D₄ ensure that Q₁ remains "off" until the pulse amplitude across C₁ exceeds about 3 volt. A rounded top pulse of about 4.7 volt amplitude is formed across C₁ if the base connection to Q₁ is opened. A square pulse of about 24 volt nominal amplitude is produced at the collector of Q₁. This form of trigger generating circuit has the added advantage that it has a high degree of immunity against noise on the input timing line.

Photographs of some waveforms relevant to the input circuit have been taken with a Tektronix Oscilloscope Camera and are presented in Fig. 4. Details of the relevant traces are:

(i) Trace (a) - Input timing pulse appearing between pins 2 and 1 (pin 1 common) of P₁ (See Fig. 3) when flashing a neon connected in parallel with these pins. Note the slope change which occurs when the neon fires. The voltage decays to virtually zero after about 1 millisecond.

(ii) Trace (b) - Integrated pulse appearing as the base of Q₁. Note that after about 50 microsecond has elapsed since the arrival of the input pulse the waveform becomes clamped to approximately 3 volt below the positive supply rail for about 200 microsecond, then rises back towards the positive supply rail again.

(iii) Trace (c) - "On" pulse of about 200 microsecond duration appearing at the collector of Q₁. These fixed amplitude pulses trigger the following binary chain.

(iv) Trace (d) - Triggering pulses appearing on the diode side of C₂. These pulses are formed by differentiation and diode gating of the pulses referred to for trace (c).

4. DECADE DIVIDER

Transistors Q₂ to Q₉ and associated circuitry constitute a series connection of four binaries. Positive "on" trigger pulses are symmetrically gated to succeeding binary stages in a "collector triggering" arrangement. Diodes D₇, D₁₀, D₁₃ and D₁₈ allow

differentiating capacitors C2, C6, C10 and C14 respectively to discharge rapidly in readiness for the following trigger pulse.

Feedback diodes D15 and D16 convert the nominal divide by 16 arrangement to a divide by 10 arrangement. Initially a tendency, accentuated by capacitive loading on the collectors of Q4 and Q6, for the circuit to divide by 8 was noted. When performing as a decade divider the 8th pulse causes Q4 and Q6 to switch "off" followed momentarily by the switching "on" of Q8 which, in turn, by virtue of the feedback diodes, causes Q4 and Q6 to switch "on" again. However since it is usually a quicker process to switch a transistor "on" than switch it "off" (bring it out of saturation in this arrangement) it is possible for the "on" pulse from Q8 to be fed back to Q4 and Q6 before these transistors have time to switch "off". Under these conditions the amplitude of the pulses fed back by diodes D15 and D16 is too small to prevent Q4 and Q6 from reverting to the "off" state and remaining in that condition. If this occurs, a divide by 8 circuit results as illustrated by the waveforms sketched in Fig. 5. To overcome this problem C15 has been added to delay the switching "on" of Q8 slightly, and hence to allow Q4 and Q6 to switch "off" before the feedback trigger pulses arrive. With C15 added no further trouble with erroneous divide by 8 operation has been encountered.

The waveforms appearing on the output of the first, second, third and fourth binaries are given in the oscillograph photographs (f), (g), (h) and (i) respectively of Fig. 4. These photographs have been taken at an input pulse rate of 100 p.p.s. (output pulse rate 10 p.p.s.).

5. OUTPUT CIRCUIT

Basically the output circuit is required to provide a signal of suitable amplitude and duration for the S.F.I.M. signal detector galvanometer. The galvanometer is essentially an electromagnetic relay carrying a mirror and has the following characteristics:

Minimum Operating Voltage	16 volt
Release Voltage	14 volt
Resistance	4000 ohm
Natural Frequency	250 hertz

Recordings taken with variable width output pulses indicated that a pulse of approximately 10 millisecond duration provided a trace which could be readily resolved at the highest chart speed

(25 mm./sec. \pm 30%) and also seemed optimum from the point of view of reading the recordings. Generation of a 10 millisecond duration output pulse is performed using a monostable multivibrator triggered from the last stage of the decade divider. Transistors Q10 and Q11, and associated circuits, constitute this multivibrator. The pulse duration time for the multivibrator is given approximately by

$$T = RC \ln 2$$

$$\text{where } R = R_{34} \text{ (kilohm)}$$

$$C = C_{20} \text{ (microfarad)}$$

$$T = \text{Pulse Duration (millisecond)}$$

For $R = 68$ kilohm and $C = 0.22$ microfarad T is approximately 10 millisecond.

In order to check that the unit is operating satisfactorily a test facility has been added in parallel with the galvanometer output. This facility involves a relay and an incandescent lamp. Under test conditions the 700 ohm energising coil of the relay is connected across the output and the incandescent lamp is connected, via the relay contacts, across the supply (Refer to Fig. 2). Final transistor Q12, which acts as a switch operated by the monostable multivibrator, provides positive going "on" pulses of virtually supply voltage amplitude capable of driving either the SFIM galvanometer or the relay coil (Refer to Trace (j) of Fig. 4). Diode D5 suppresses reverse polarity inductive spikes generated by the galvanometer coil or the relay coil. Resistor R3 has been added in series with the galvanometer output to provide some measure of short circuit protection should the remote output for the SFIM galvanometer be accidentally shorted. Under test conditions the incandescent lamp flashes (of approximately 10 millisecond duration and repetition rate of either 2.5 p.p.s. or 10 p.p.s.) can be readily resolved and any irregularity in the output pulses is easily detected.

Fig. 6(a) is a sample of a recording of the divided timing pulses taken with a SFIM Recorder. When the input frequency changes from 25 p.p.s. to 100 p.p.s., the divided pulse rate changes from 2.5 p.p.s. to 10 p.p.s.. However the number of input pulses which elapse before the divider provides an output subsequent to the frequency change will depend on the state of the count in the decade divider at the change. The location of the change point can be ascertained quite accurately. Fig. 6(b) illustrates, using an

exaggerated scale, a typical arrangement of SFIM timing pulses in the vicinity of the frequency change. Pulses, A, B and C are interspaced by $\frac{1}{2.5}$ second (designated 4T) and pulses, D, E and F are interspaced by $\frac{1}{10}$ second (designated by T). Obviously the change occurs somewhere between pulse C and pulse D. For the purposes of the following analysis define the following:

aT = time interval between frequency change and pulse D.

bT = time interval between pulse C and pulse D.

n = number of input pulses at the repetition rate of 100 p.p.s. which occur between frequency change and pulse D.

It follows that

$$bT = \frac{4(10-n)T + nT}{10}$$

$$= T \left(4 - \frac{3n}{10} \right)$$

$$b = 4 - \frac{3n}{10}$$

$$n = \frac{10(4-b)}{3}$$

$$a = \frac{4-b}{3}$$

The last expression enables the frequency change point to be located quite accurately.

6. CONSTRUCTIONAL DETAILS

The complete divider circuit (as drawn in Fig. 3) has been mounted on a plug-in 8.5 inch by 4 inch printed circuit card as illustrated in Fig. 7. Details of the printed circuit layout, as viewed from the underside of the board, are illustrated in Fig. 8. The printed circuit unit has been potted on both sides of the card using Silastic (Silicone Rubber) RTV589 potting compound of Dow Corning manufacture.

7. PERFORMANCE FIGURES

Current Demand. The total current drawn for a 100 p.p.s. input is 22 mA at 24V supply with check circuit inoperative.

Supply Voltage Range. The divider circuit operates satisfactorily down to 10V. The upper limit would depend on transistor ratings and has not been taken higher than 32V, the highest voltage

of interest. Note however that the SFIM galvanometer will not operate below about 20 volt supply.

Supply Impedance. With the check facility inoperative the circuit performs satisfactorily with up to 260 ohm (unbypassed) in the supply line.

Input Line Capacitance. The capacitance across the input timing line affects the shape of the input pulse. The Table below indicates the value of input line capacitance which is required to upset the operation of the divider.

SUPPLY VOLTAGE	30V	25V	20V	15V	10V
INPUT LINE CAPACITANCE	0.09 μ F	0.09 μ F	0.10 μ F	0.10 μ F	0.11 μ F

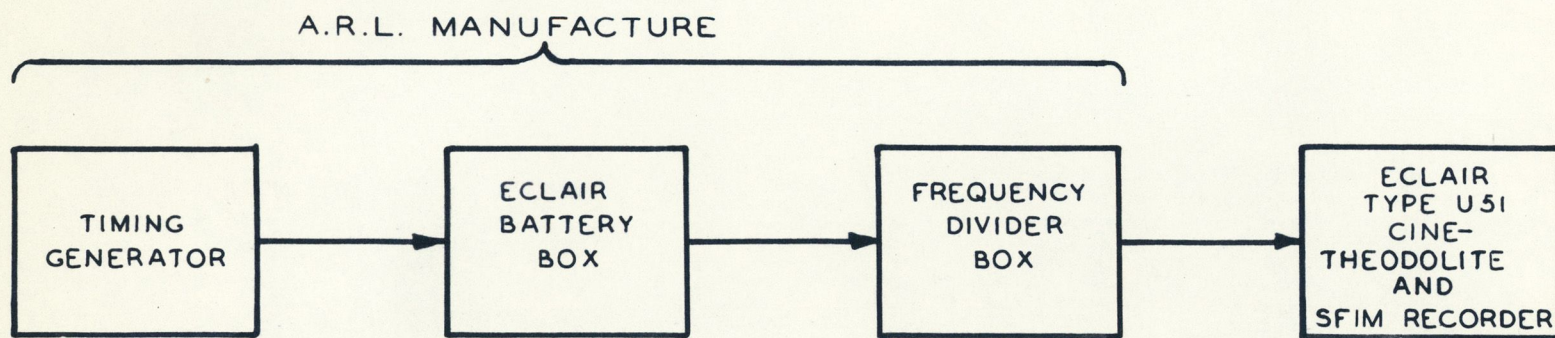
Temperature. Satisfactory operation of the divider circuit has been obtained up to 90°C (the highest temperature obtainable from the heating apparatus used).

REFERENCES

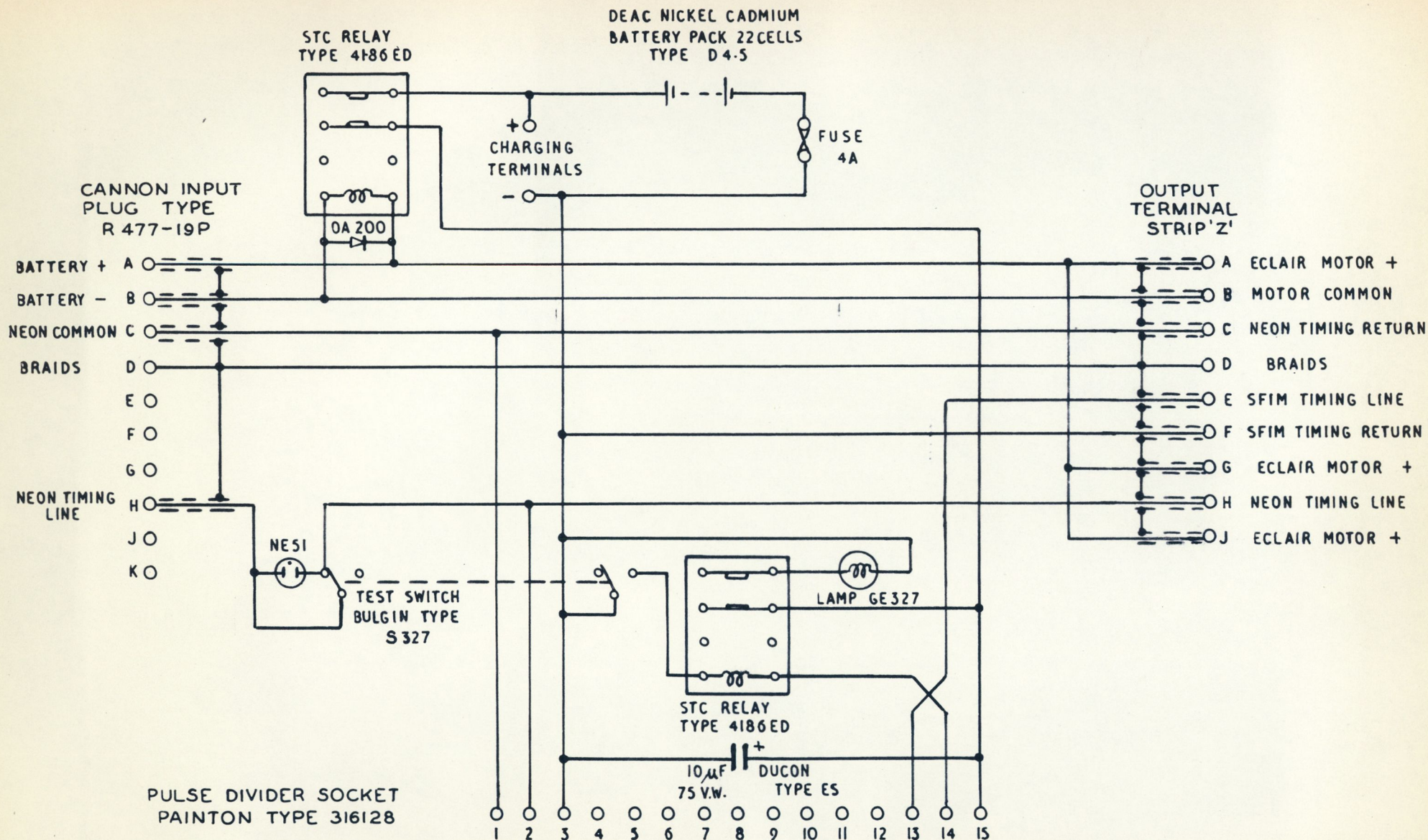
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POSTAL ADDRESS:-

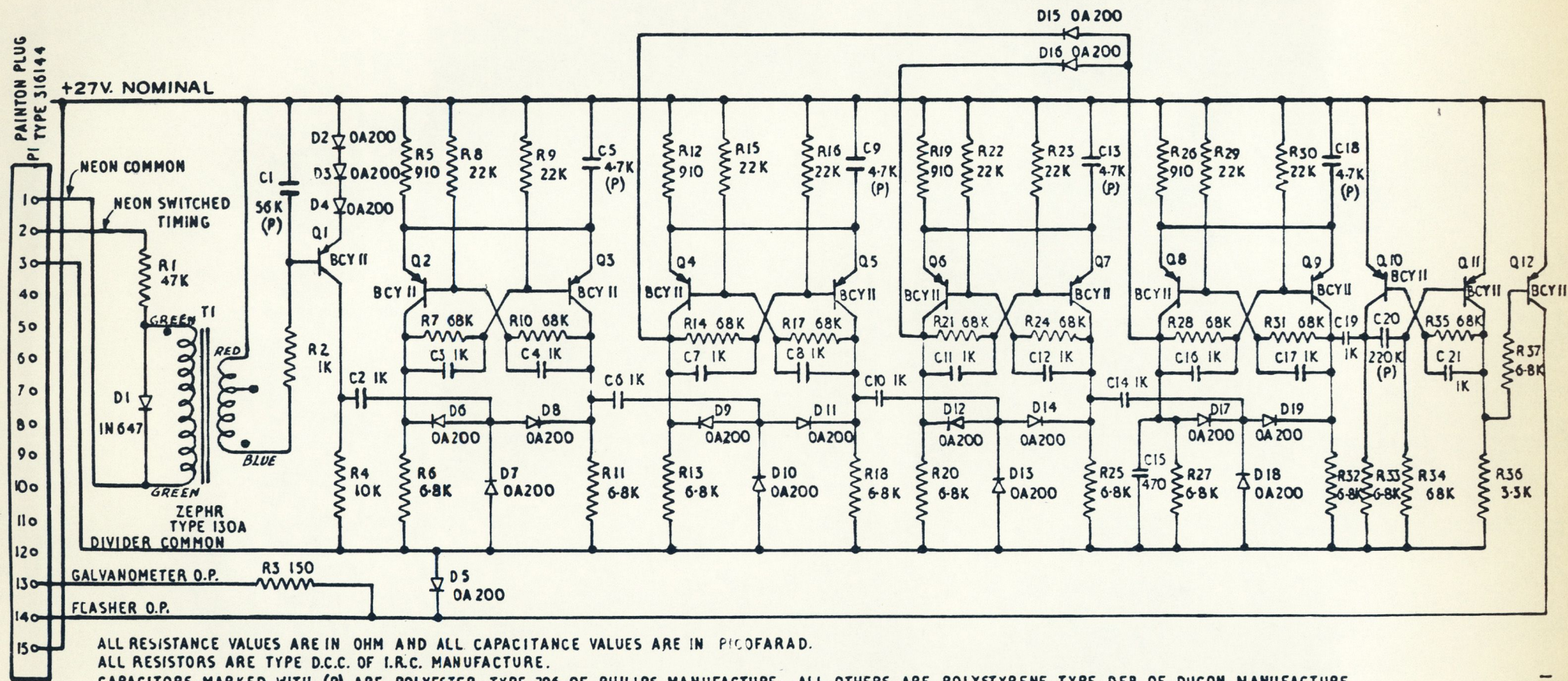
The Chief Superintendent,
Aeronautical Research Laboratories,
P.O. Box 4331, Melbourne, Victoria. 3001.



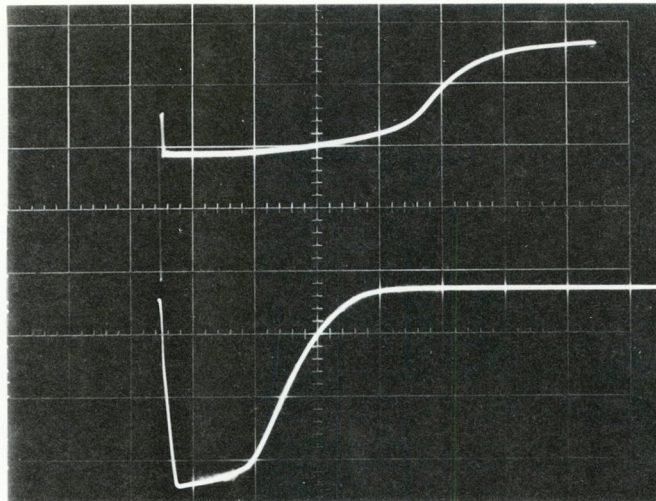
BLOCK SCHEMATIC OF MISSILE TRACKING SYSTEM USING ECLAIR
CINETHEODOLITE



DIVIDER BOX INTERCONNECTION DIAGRAM



COMPLETE CIRCUIT OF PULSE FREQUENCY DECADE DIVIDER



(a) UPPER TRACE

INPUT TIMING PULSE
(AT PIN 2 OF P1)

HORIZ. SCALE 0.2mSEC./DIV.

VERT. SCALE 50V/DIV.

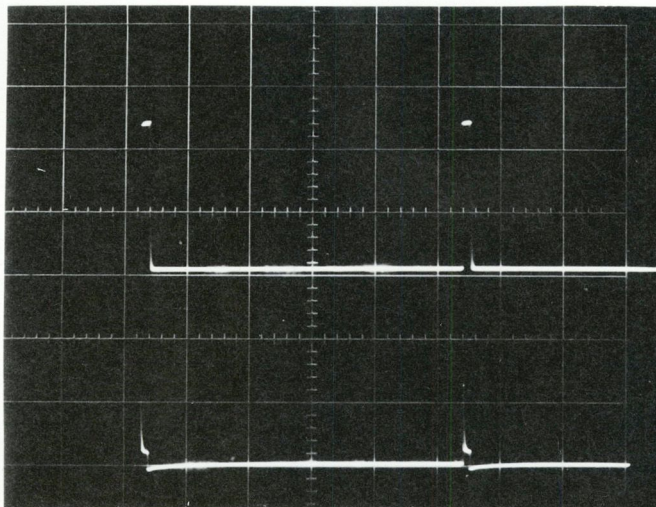
(DIV. = LARGE DIVISION)

(b) LOWER TRACE

INTEGRATED PULSE
(AT BASE OF Q1)

HORIZ. SCALE 0.2mSEC./DIV.

VERT. SCALE 1V/DIV.



(c) UPPER TRACE

PULSE FORMED AT
COLLECTOR OF Q1

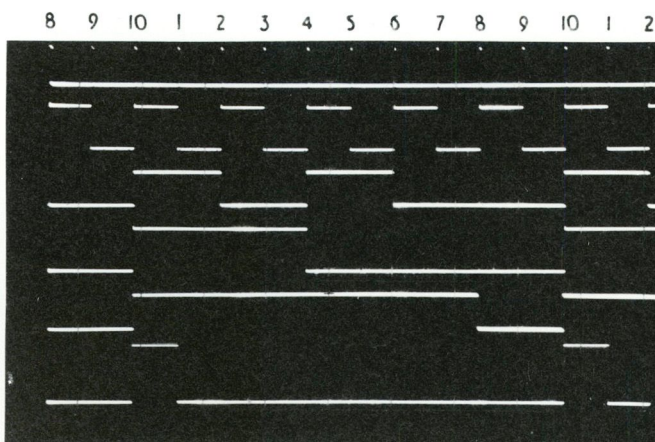
HORIZ. SCALE 2mSEC./DIV.

VERT. SCALE 10V/DIV.

(d) LOWER TRACE

DIFFERENTIATED PULSE
(DIODE SIDE OF C2)

SCALES AS FOR (c)



PULSE RATE = 100 p.p.s.

(e) COLLECTOR OF Q1

(f) COLLECTOR OF Q3

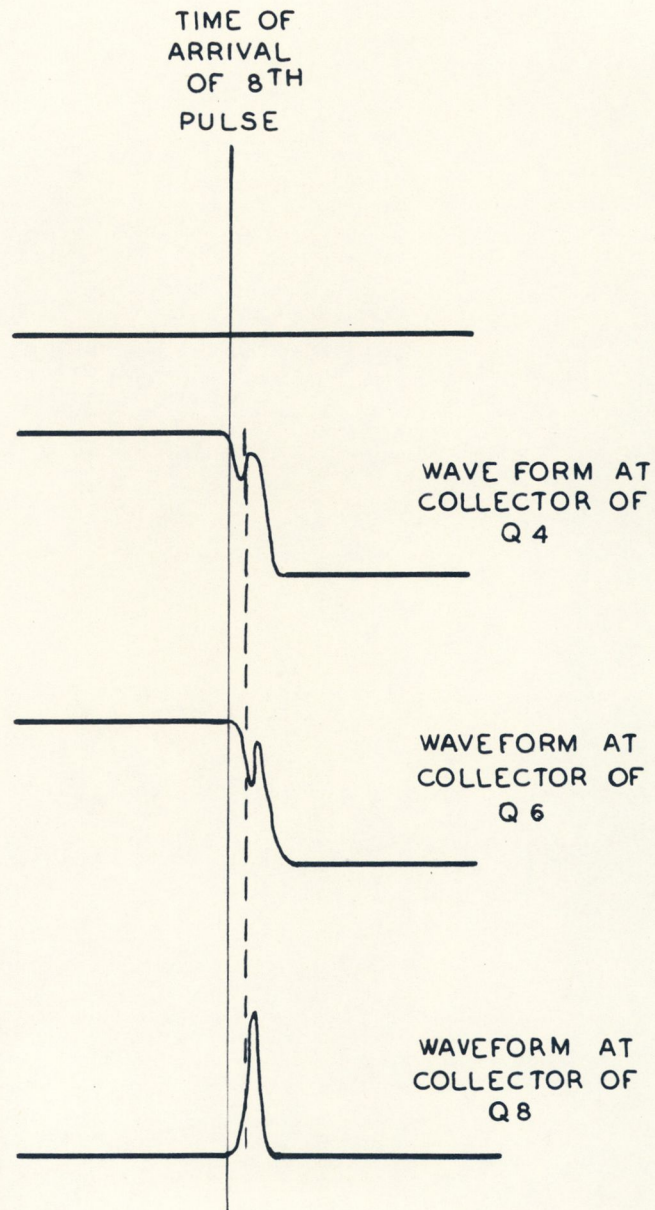
(g) COLLECTOR OF Q5

(h) COLLECTOR OF Q7

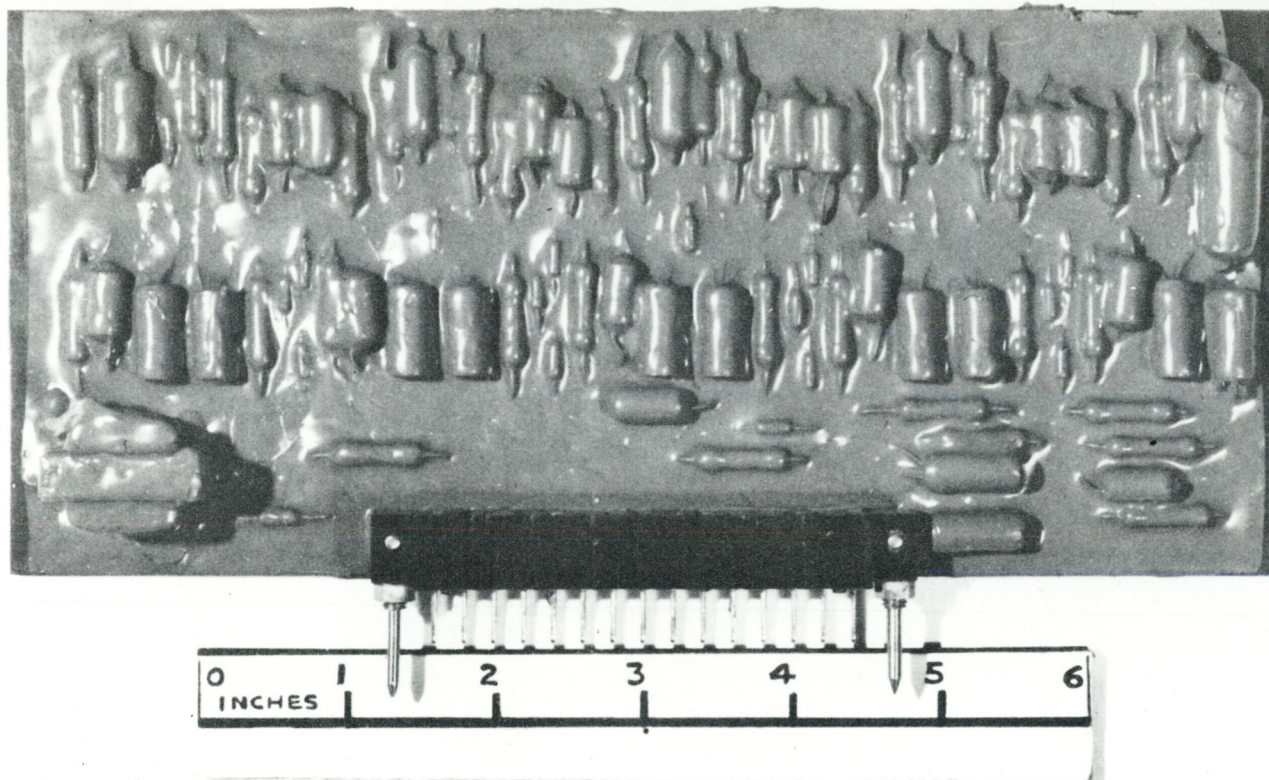
(i) COLLECTOR OF Q9

(j) COLLECTOR OF Q12

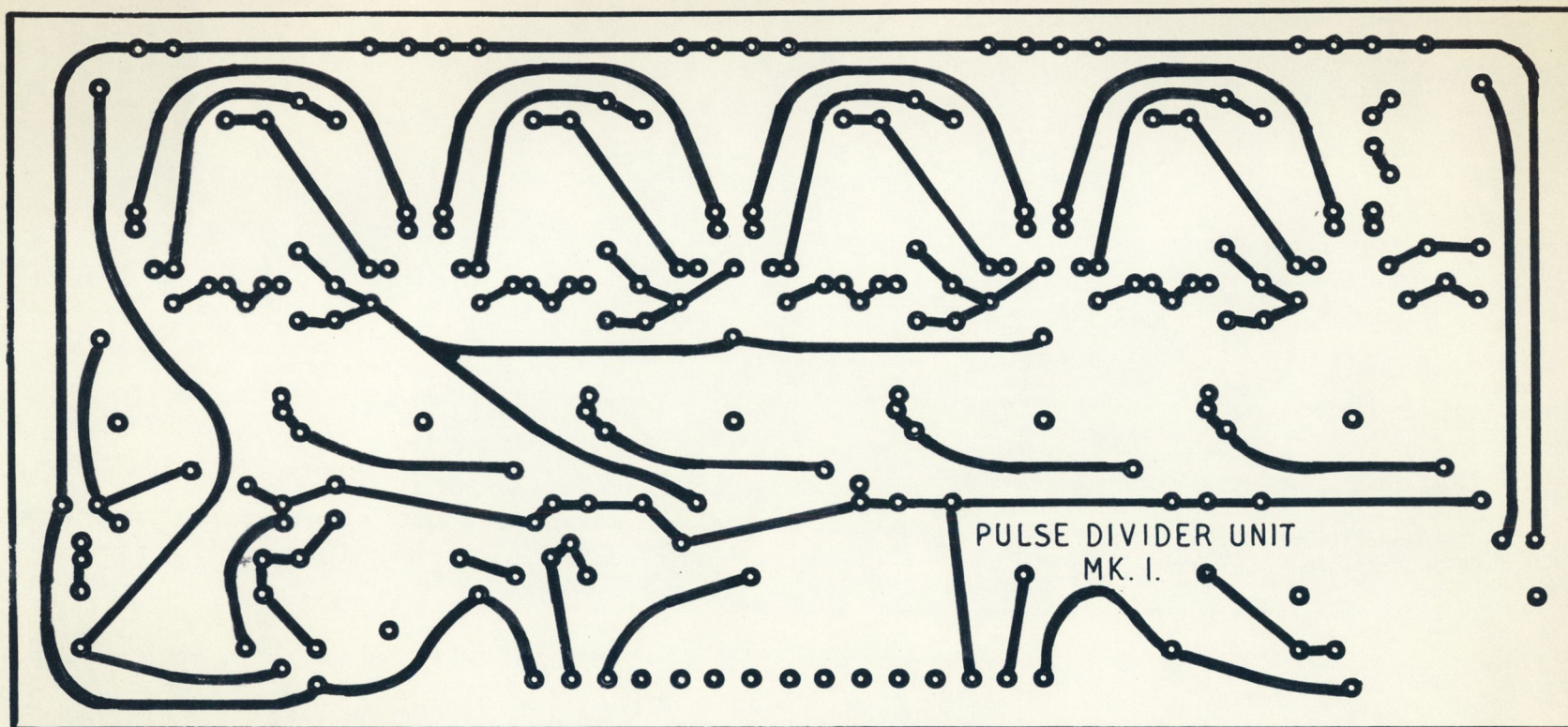
OSCILLOGRAPH WAVEFORMS



RELEVANT WAVEFORMS FOR DIVIDE BY 8
CIRCUIT
(EXAGGERATED TIME SCALE)



PULSE FREQUENCY DIVIDER CIRCUIT BOARD



PRINTED CIRCUIT LAYOUT OF PULSE FREQUENCY DIVIDER