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AIRCRAFT ENGINE SPEED AND FUEL FLOW SIGNAL CONDITIONER WITH DIGITAL OUTPUT

by

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Summary

Engine speed and fuel flow rate sensors typically provide outputs in the form of a pulse train with repetition rate proportional to the measurand. Digitization of such data is readily accomplished by counting the number of pulses received per unit time. A conditioner which produces such digitization is described. It has the special property that no pulses are ever missed when the contents of the counter are transferred to associated data recording equipment. Thus the conditioner can be used for accurate totalizing of engine revolutions or fuel consumed over long periods.

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1. INTRODUCTION

An investigation into the feasibility of determining the condition (or "health") of military aircraft engines from in-flight recordings of engine performance parameters is currently being undertaken by these laboratories on behalf of the Royal Australian Air Force. Initial evaluation studies are to be performed on a Viper engine in a Macchi aircraft fitted with data acquisition equipment which has been manufactured recently.

It is intended that the following eight parameters be recorded initially:

1. Engine intake total pressure.
2. Engine intake total temperature.
3. Engine speed.
4. Fuel flow rate.
5. Exhaust gas total pressure.
6. Exhaust gas total temperature.
7. Ambient static pressure.
8. Ambient pitot pressure.

Using specially developed data acquisition equipment[1] recording is to be performed in serial digital format on a cassette tape. Of the eight parameters listed above for recording, all except engine speed and fuel flow rate are most conveniently transduced initially to analogue voltage signals (voltage level proportional to quantity being measured) via sensors together with suitable signal conditioners. Conversion of such analogue voltage signals to digital form is achieved using a conventional analogue to digital converter included in the data acquisition equipment.

Sensors for engine speed and fuel flow rate on the other hand typically provide outputs in the form of a variable rate pulse train or continuous signal with frequency proportional to the quantity being measured. In the present engine application the number of sinewave "pulses" received per unit time from an engine driven generator provides a measurement of engine speed. The rate of fuel consumption in the aircraft is initially converted to an analogue rotational speed of an impeller placed in the fuel flow path. The rotational speed of the impeller is sensed using a pick-up coil to detect the passing of a magnet fitted to the impeller. Hence the number of pulses received per unit time from the pick-up coil provides a measurement of the fuel flow rate.

It follows therefore that the basic sensors for engine speed and fuel flow rate provide analogue frequency outputs. Generally conversion of analogue frequency to digital form can be performed in two ways:

(1) The frequency can be converted to an analogue voltage as in conventional tachometer circuits which provide a meter movement or similar analogue readout. The analogue voltage can then be converted to digital form using an analogue to digital converter.

(2) The frequency can be converted directly to digital form by counting the number of cycles which occur in a fixed time interval.

When the frequency output from the sensor is very low, improved short term resolution may result if system (1) is used, but could also be achieved with system (2) if a frequency multiplier were employed. To achieve adequate response to speed changes it is not normally possible with system (1) to use a filter capable of producing a smooth output at low pulse rates. If the frequency output is sufficiently high improved accuracy and speed of response will normally result if system (2) is used. Furthermore by counting all incoming pulses, system (2) can be used to achieve excellent long term accuracy, or can be used as a totalizer to measure engine revolutions or fuel consumed respectively if individual pulse counts are summed over the prescribed totalizing period. Such a summation can be conveniently performed with the aid of a ground station digital computer which would normally be used to analyse the recorded data.

After due consideration of the factors mentioned above, system (2) has been adopted for engine speed and fuel flow rate measurement.

Although the data recording requirements for engine health monitoring formed the impetus for the development of the engine speed and fuel flow rate conditioner described in this document, some consideration has been given to more general uses. In particular, in a system[2] of general purpose airborne data acquisition developed at these laboratories, there is a need to digitize a variety of signals which are sensed as analogue frequencies. Further, in that case the digital conversion rate is selectable over a wide range to meet signal bandwidth requirements. Very little additional circuit refinement has been necessary to accommodate all the requirements of this general purpose system.

2. CONDITIONER REQUIREMENTS

The associated data acquisition equipment,[1] named 16 CAD Recorder (from "sixteen channel analogue and digital recorder") will accept up to 12 analogue inputs and up to 4 digital inputs. Each input is allocated a 4-bit binary address, equivalent to 0 through 15 decimal, where addresses 0 to 11 are allocated for analogue inputs and addresses 12 to 15 for digital inputs. Using a plug-in read only memory (ROM)[1] any desired channel sampling sequence within a frame of data can be arranged by programming the ROM with the appropriate address sequence. Each frame of data accommodates 22 samples. For the present study the frame repetition period has been set to 1 second. Thus if a particular address occurs twice per frame than 2 samples of data will be taken per second from the corresponding input. Initially the ROM has been programmed to allow 10 channels to be sampled once per second and 6 channels twice per second. As only 8 channels of data are to be recorded initially, 8 of the available 16 channels are spare for extension if required.

Selection of analogue channels is performed internally in the 16 CAD Recorder so that each hard-wired analogue input has a uniquely defined address. To enable selection of a digital channel the four line address is taken externally to the conditioning equipment and must be decoded there. Transfer of the two digital outputs (corresponding to engine speed and fuel flow rate in the present instance) from the conditioner to the 16 CAD Recorder must take place on the same parallel input bus (requiring one wire per information bit) so that multiplexing of the respective digital outputs, within the conditioner, under address control, is essential. Further, it has been decided that the incoming digital data bus also carry the output of the analogue to digital converter (ADC), incorporated in the 16 CAD Recorder, when analogue inputs are addressed. Thus the data bus must allow data transfer in either direction, hence the digital outputs from the engine speed and fuel flow rate conditioning circuits must switch to the high impedance state when their respective inputs are not addressed.

One major advantage of the two way bus is that, without the need for a separate multi-line output, it can be readily coupled to a digital monitor[3] which by simple address selection will display the digitized output corresponding to any data channel (either analogue or digital). Such a display is very useful for pre-flight checkout and calibration.

The study of engine condition requires that small changes in performance be detectable. Hence recording of engine performance parameters with high accuracy is a requirement. At present the recording resolution is limited to 1 part in 256 by the 8-bit recording word length used in the 16 CAD Recorder. However as it is possible that increased resolution may be a future requirement it is desirable that the engine speed and fuel flow rate conditioner be not limited to 8-bit capability.

Crystal controlled timing is incorporated in the 16 CAD Recorder. By utilizing control outputs from the recorder for timing, the conditioner need not internally generate accurate count time intervals.

For the Macchi aircraft, engine speed is displayed to both pilots by cockpit indicators which derive their input from a Smiths Type KGA0701 tacho-generator driven by an accessory gearbox at $\frac{87}{286}$ (approximately 0·304) of engine main shaft speed. The two pole generator provides a three phase output of frequency proportional to engine speed. It has been decided that the generator be used as the engine speed sensor.

The engine speed range over which recording is required for engine condition investigation is 50 to 105% where 100% engine speed is nominally 13,800 revolutions per minute (RPM) or 230 hertz (Hz). Thus the generator frequency range of interest is 35 to 73·5 Hz (allowing for the accessory drive gearbox reduction).

Because the cockpit indicators load the tacho-generator close to its capacity the current available for the conditioner is fairly low (about 10 milliamp root mean square (RMS) from each phase would be acceptable). The generator output voltage between phases is nominally 16 volt RMS at 100% shaft speed and varies almost linearly with shaft speed. One phase of the generator is connected to aircraft ground.

Fuel flow rate for the engine is sensed using a Faure Herman Type RCM 128PA rotating impeller type transmitter which provides a pulse rate output proportional to fuel flow rate. The output of the transmitter is taken via an amplifier to cockpit indicators which provide (for each pilot) meter display for instantaneous fuel flow rate and digital readout for total fuel consumed. Because the amplifier does not provide a conveniently accessible output signal with frequency equal to that of the transmitter output, it has been decided that a fuel flow rate signal be derived directly from the transmitter output by using a parallel take-off on the cabling. One disadvantage of taking a pulse output from the transmitter is that the level is relatively low. However if the conditioner is to be made general purpose, suitable for similar use in other aircraft, then the development of a conditioner capable of operating on the basic sensor output is very desirable. The characteristics of the transmitter are as follows:

(i) The fuel flow rate range is 160 to 4,000 pound per hour (72·6 to 1,814 kilogram per hour).

(ii) The pulse output factor is 128 pulses per pound of fuel (282·1 pulses per kilogram of fuel). Hence the pulse rate range for the above fuel flow rate range is 5·7 to 142·2 Hz. The transmitter has a tapered adaptor which may be adjusted to provide the same output for fuel of different density.

(iii) The pick-up coil has a resistance of 3,500 ohm approximately.

(iv) The "low" side of the transmitter output is connected to aircraft ground via the amplifier.

(v) The transmitter output takes the form of a double unsymmetrical pulse (Sec. 4.1.1) with larger negative amplitude. Peak to peak amplitude is approximately proportional to pulse rate and ranges from about 30 to 1,000 millivolt peak to peak over the specified fuel flow rate range.

For the present engine condition study the fuel flow range of interest is nominally 500 to 3,500 pound per hour (227 to 1,588 kilogram per hour). However, for increased versatility, it is highly desirable that the conditioner accommodate the full fuel flow range of the transmitter.

Since the outputs from both the engine speed and the fuel flow rate sensors are referenced with respect to aircraft ground it is essential that the respective aircraft ground inputs be not joined together within the conditioner by connecting to an internal common, as in that case excessive noise may be developed due to the resulting ground currents. Some form of input isolation is therefore essential.

To prevent significant loss of pulse amplitude at the fuel flow transmitter output the conditioner must not significantly load the pick-up coil (3,500 ohm resistance).

Very precise engine speed measurement can be achieved provided no extraneous noise pulses are counted. Similarly the speed of the impeller used in the fuel flow transmitter can be measured very accurately, but the overall accuracy is limited by the fuel flow rate to impeller speed conversion accuracy, which the manufacturer states to be better than 1%. Extreme care needs to be taken to prevent extraneous noise pulses from being mixed with sensor output pulses in such a way that erroneous output readings result.

It is highly desirable that the engine recording system be capable of counting and recording (as a series of sub-totals for instance) all incoming pulses from the sensors so that very accurate readings of totalized fuel consumed or totalized engine revolutions, over a longer period than just a single frame repetition period, be achievable. Such a capability is even more important if the conditioner is to find general purpose use for "frequency" type data sampled at higher rates.

3. GENERAL DESCRIPTION OF SYSTEM OF DIGITIZATION USED IN THE CONDITIONER

A block schema of the system developed for engine speed and fuel flow rate digitization is drawn in Fig. 1. Basically the conditioner may be divided into two major circuits:

1. Input signal conditioner.
2. Frequency to digital converter.

In the case of hardware manufactured for engine condition evaluation studies on the Macchi aircraft, the major circuits have been constructed on separate printed circuit boards. The input signal conditioner is designed to meet the specific requirements of the particular sensors used. If a different set of sensors with pulse rate outputs is to be used in other applications, the input signal conditioner may have to be altered. The frequency to digital converter, on the other hand, is a dual channel general purpose digitizer which would find universal use as a digital converter for input data with frequency proportional to the quantity to be measured.

The tacho-generator (Fig. 1) used for engine speed sensing generates a three phase sinusoidal output of 73·5 Hz (Sec. 2) for the maximum speed of interest (105% speed) where 100% speed is equivalent to 13,800 RPM. Insufficient short term resolution (1 in 73·5 or 1·4% of full scale for a 1 second count period) would result if only 1 pulse per cycle of the input signal were counted. However by sensing the combined number of zero crossings (say) per second for all output phases the input pulse rate can be effectively increased by a factor of 6. Provided the phases are balanced, as is very closely true for the Viper engine speed indicating system, the 6 pulses per cycle of the input should be very nearly equi-spaced in time.

A delta connection of optical isolators (Fig. 1) is used to generate 6 output pulses per cycle of the three phase input from the tacho-generator. Resolution then becomes 1 part in 441 or 0·22% of full scale for a 1 second count period. Sufficient current can be derived from the generator output to meet the input requirements of the isolators. The optical isolators provide very good isolation between the conditioner "common" and the inputs, one phase of which is connected to aircraft ground, and allow the outputs to be readily summed together (shown diagramatically with the OR gate of Fig. 1).

Greatest sensitivity to extraneous noise occurs at the times of switching of the optical isolators. Improved noise immunity results if a monostable multivibrator is used at the output of the engine speed input conditioner. While the multivibrator output pulse is in the "true" state any additional switching transitions at its input will not produce additional switching transitions at the output.

In effect the engine speed input signal conditioner produces, at its output, a train of TTL (transistor–transistor–logic) compatible pulses at a repetition rate equal to 6 (3, 2 and 1 available as alternatives) times the generator output frequency.

The fuel flow rate transmitter output is taken to the input of a differential voltage comparator set to switch at a slightly negative input voltage, so that for signals of lowest amplitude and frequency, switching will occur at a point on the input waveform where the slope is high. Because the transmitter output is unsymmetrical only one pulse is generated per cycle of the input. Short term resolution (for 1 second count period) is 1 part in 124·4 or about 0·80% of full scale where full scale is required to correspond to 3,500 pound of fuel per hour (Sec. 2). Once again improved noise immunity is achieved using a monostable multivibrator at the output of the fuel flow rate input conditioner.

Whenever the 4-line address input to the conditioner corresponds to the engine speed or fuel flow rate input address a reading of the respective digitized data is required for recording using the 16 CAD Recorder. In order to read the appropriate data and transfer them to the output data bus the incoming address is compared with the engine speed input address (address A) and the fuel flow rate input address (address B) for equality via the digital comparator used in the address decoder (Fig. 1). Address A and address B are presettable in the address decoder. When equality of the input address with address A or address B occurs the respective output (GATE A or GATE B) will switch to the true state and will result in the appropriate data being transferred to the output bus.

Conversion of the input signal conditioner pulse rate output to digital form, and transfer of the digital information to the data bus, is next accomplished with the frequency to digital converter (Fig. 1).

A command to convert (CTC) signal is internally generated in the 16 CAD Recorder and is used to initiate conversions in the ADC within that recorder when analogue inputs are addressed. As indicated earlier (Sec. 2) 22 inputs are addressed per second (the data frame repetition period). Each time an address advance takes place a negative going pulse (Fig. 1) of $\frac{1}{360}$ second (2·78 millisecond) duration is generated at the CTC output from the 16 CAD Recorder. Twenty of the CTC pulses received in a 1 second data frame are spaced $\frac{1}{20}$ second (50 millisecond) apart in time, and the remaining two (corresponding to analogue input addresses 1 and 2) are equispaced at $\frac{1}{60}$ second

intervals within one of the $\frac{1}{20}$ second intervals (refer to Sec. 4.1.3 and Fig. 6). The digital information on the data bus is read and temporarily stored in the 16 CAD Recorder some time after the CTC pulse switches high but before a new input address is generated. Transfer of information from the engine speed and fuel flow rate conditioner to the output bus takes place at the time of the positive transition of the incoming CTC pulse but only when the incoming address corresponds with address A or address B respectively. Initially the ROM in the 16 CAD Recorder has been programmed such that the engine speed address (address A) is received twice per second (at a regular 0·5 second repetition period) and the fuel flow rate address (address B) is received once per second.

The accuracy and the stability of the count time interval for the frequency to digital converter is directly related to the accuracy and the stability of the CTC pulse timing. The CTC pulses from the 16 CAD Recorder are internally generated in that recorder using a stable crystal oscillator[1] with frequency divider. Over the temperature range −30 to +70 degrees Celsius the measured frequency stability of the crystal oscillator is better than 0·017%.

Counting of INPUT A and INPUT B pulses (Fig. 1) from the input signal conditioner is performed by 12-bit binary counters (one for each input) in the frequency to digital converter. Thus these counters have a maximum resolution of 1 part in 4,096. However the 16 CAD Recorder in its present form will accept 8-bit words only but, as indicated in Sec. 2, better resolution capability is desirable (mainly to allow the conditioner to be used in general purpose applications where additional resolution may be required, but also to make it compatible with the 16 CAD Recorder if ever that recorder were updated to provide extra resolution).

The counters have latching capability and tri-state outputs. Normally incoming pulses are transferred without delay to the counters, but if a command-to-read the counter is received at the same time as an input pulse (from the relevant input signal conditioner) then the input pulse will be delayed till the read sequence is over. Thus no counts are "lost" and ambiguity cannot occur if read command and input pulse signals are synchronous (or nearly synchronous) in time.

Each time a CTC pulse is received by the frequency to digital converter the following sequence of signals is generated by the read signal generator (Fig. 1):

(i) A LATCH signal which causes the counter contents to be loaded into the latches;

(ii) A CLEAR signal which causes the counter contents to revert to the zero count state;

(iii) A COINCIDENCE TEST GATE signal which establishes a short time interval during which any input pulse received will be deemed to be "coincident".

Whenever the GATE A or GATE B outputs switch low, the output bus will be connected to the outputs of the respective latches. Latching always takes place when a CTC pulse is received but the latch/reset sequence only takes place when the appropriate gate signal (GATE A or GATE B) is low.

The counter read controller effectively causes latch and reset signals to be transferred to the counters (included in Digitizer A or Digitizer B as indicated in Fig. 1) and causes the relevant counter input to be delayed if the negative transition of an input pulse occurs within about 1·2 microsecond after the positive transition of the CTC pulse which initiates the read sequence. The counter read controller, the coincidence controlled delay circuit and the 12-bit counter/latch effectively constitute a Digitizer (A or B respectively). Identical circuits are used for each Ditigizer, in this case two. The Read Signal Generator on the other hand is a common requirement of all digital channels and would not have to be repeated if more channels were added, except that some buffers would be required to increase the drive capability.

Each digital channel is capable of handling input pulse rates in excess of 700 KHz (refer Sec. 4.2), but for 12-bit operation at least 170 readings would have to be taken per second to prevent counter overflow. For an 8-bit system at least 2,720 readings per second would be required to accommodate a 700 KHz input rate. The maximum permissible number of digital conversions per channel per second is given by $\frac{700{,}000}{\text{No. of Digital Channels}}$ (i.e. a rate of 350 KHz for a two channel system). A conversion rate higher than the input pulse rate is quite permissible. In that case, however, the readings would be 0 or 1 but the totalized count over a longer time interval would still be accurate.

Power for the aircraft engine speed and fuel flow rate digitizer (including the input signal conditioners as indicated in Fig. 1) is derived from the aircraft 28 volt DC supply via a DC to DC converter which provides a single +5 volt output. In addition the +5 volt output supplies power for the Digital Signal Monitor (Fig. 1).

4. DETAILED DESCRIPTION OF CIRCUITS USED IN THE CONDITIONER

4.1 Input Signal Conditioner

As indicated in Sec. 3 the input signal conditioner has been manufactured in the form of a single plug-in board. Complete circuit details are given in Fig. 2 and component layout information is given in Fig. 3. For details on components and on the system of component labelling used in this report refer to Appendix I.

The input signal conditioner may be subdivided into three sections:

(i) Fuel flow input conditioner,

(ii) Engine speed input conditioner,

(iii) Input address decoder.

These sections will now be considered in turn.

4.1.1. Fuel Flow Input Conditioner

The fuel flow input conditioner comprising devices Q1, Q2, Q3A, Q4A and associated components (Fig. 2) ideally converts the fuel flow rate transmitter output into a high level noise-free TTL compatible output. Relevant waveforms for the conditioner are given in Fig. 4.

Typically the input takes the form indicated in waveform 1 (Fig. 4). The peak excursion below the "zero volt" level is normally greater than the excursion above it and the difference becomes accentuated at the higher frequencies. The peak to peak amplitude is approximately proportional to frequency and has a value of about 30 millivolt peak to peak at the minimum frequency (about 5·7 Hz corresponding to a fuel flow rate of 160 pound per hour) of the fuel flow rate transmitter.

A balanced differential input comparator incorporating Q1 and associated components converts the relatively low level input signal to one which switches abruptly between two levels (0 and 5 volt nominally). The input stage functions as follows:

(i) By using coupling capacitors C1 and C2 (one in each input line) shifting of the DC operating point due to DC common mode input signals is prevented, and operation from a single supply (+5 volt) is made feasible.

(ii) By using a balanced differential input (taking special care to balance R4 and R5) some level of rejection of AC common mode noise signals, having frequencies within or outside of the band of interest, is provided.

(iii) By using a simple low pass input filter incorporating components C3, R6, C4 and R7 any differential mode (i.e. superimposed on signal) noise signals having frequencies higher than the maximum frequency of interest (about 142 Hz) are attenuated.

Resistor R2 is selected to provide a DC differential input equivalent to 10 millivolt relative to the input offset voltage and set the comparator switching level to −10 millivolt. Because of this shift in switching level the Q1 comparator output is biased to the low state in the absence of input signals. Furthermore the switching point relative to the fuel flow rate transmitter output for low rates of fuel flow is one where the slope is significantly higher than the zero volt level.

At low fuel flow rates where the amplitude and frequency of the input signal are relatively low multiple transitions, as in waveform 2 (Fig. 4), will be noticeable each time the input signal passes through the switching threshold. To maintain input balance the use of positive feedback to reduce this effect has been avoided.

Decoupling of the first comparator stage is accomplished using components R9 and C5.

Multiple transitions at the output of the first comparator Q1 are "smoothed" out using the low pass filter formed by components R10 and C6. The filtered output signal takes the form indicated in waveform 3 (Fig. 4) and becomes the input to the second comparator comprising Q2 and associated components. In addition the second comparator incorporates positive feedback via C7. With this circuit arrangement the output of the second comparator (waveform 4 of Fig. 4) is free from additional switching transitions.

As an alternative to the differential input comparator a linear integrator could have been used. The output of the integrator would probably be relatively constant over the frequency band of interest. One possibility would be to use a single ended input stage (of low current consumption) powered from (but suitably decoupled from) the aircraft 28 volt supply and return the supply current via the transmitter "low". Care would have to be exercised to prevent injection of excessive noise signals into the transmitter output. A high level differential input stage would be required after the single ended stage. Alternatively a differential input linear integrator could be used in place of the first comparator. Although the integrator input may have advantages in applications where there is considerable noise (at the higher frequencies) mixed with the input signal, it has not been considered necessary in the present instance.

A "negative" (a transition from high to low level) pulse is transferred via C9 and gating diode CR2 to the input of the monostable multivibrator Q4A each time the output of the second comparator switches from high to low.

Because the input signal from the transmitter does not have its two zero crossings per cycle equispaced in time, only one pulse is transferred to the output per cycle. If, however, an input were derived from a sensor which produced a signal having zero crossings equispaced each half cycle, improved short term resolution would result if two output pulses were generated per cycle of the input. NAND gate Q3A may be used to invert the second comparator output and provide the additional trigger pulse for the monostable multivibrator. In that case terminal posts TP1 and TP2 would be linked.

The minimum repetition period of the fuel flow rate signal in the range of interest is about 6·9 millisecond (corresponding to a frequency of 142·2 Hz for a fuel flow rate of 4,000 pound per hour). Monostable multivibrator Q4A is connected in a non-retriggerable mode and when triggered will be totally immune to any extraneous noise pulse received at its input for the duration of the output pulse. The duration of the output pulse (waveform 5 of Fig. 4) has been set to 6 milliseconds which is a little shorter than the minimum repetition period of the fuel flow rate signal in the range of interest.

Improved immunity to input noise results from the use of the monostable multivibrator as the input conditioner is more susceptible to noise received just prior to or just after the normal switching times of the first comparator. Further improvement would result if two output pulses were generated per cycle of the input as a "noise immunity" time band would then be effectively generated for both positive and negative transitions of the first comparator.

Either a positive going or a negative going (from a normally high to a low state) monostable multivibrator output pulse may be taken to OUTPUT B by connecting TP4 to TP3 or TP5 respectively.

The conditioner has been tested for the rejection of common mode signals with frequencies in the band 5 to 250 Hz. For an input of 30 millivolt peak to peak at 5 Hz, the measured worst case common mode rejection occurred at 100 Hz, at which frequency the conditioner could tolerate a common mode signal 37 decibel in excess of the signal.

In measuring applications for which the fuel flow input signal common floats with respect to the conditioner common it is advisable to connect these commons together. A link (Fig. 2) may be conveniently added to the input signal conditioner printed circuit to allow such connection.

4.1.2 Engine Speed Input Conditioner

The engine speed input conditioner comprising devices Q5 to Q16, Q3B to Q3D, Q4B and associated components (Fig. 2) ideally converts the three phase tacho-generator output into a train of regularly spaced noise free pulses which are TTL compatible.

The three phase sinusoidal output from the tacho-generator is illustrated in waveforms 6, 7 and 8 of Fig. 5. At 100% engine speed the phase to phase output of the generator (loaded with the cockpit indicators) is 16 volt RMS approximately and the generator frequency is 70 Hz approximately. The range of engine speed of interest (Sec. 2) is 50 to 105% (35 to 73·5 Hz output frequency range). Generator output voltage is approximately proportional to speed.

Optical isolators (Q5, Q6, Q9, Q10, Q13 and Q14) are connected in series with resistors in a push/pull arrangement across each phase. R19 and R20 limit the current drawn from the generator by the phase A-B isolator circuit (connected between phase A and phase B) and similarly for the other two isolator circuits. The maximum current drawn from each phase has been found by

measurement to be 9 milliamp RMS (at 105% engine speed). The light emitting diode incorporated in the Q5 isolator conducts on the positive excursions of the phase A to phase B input voltage and that in Q6 conducts on the negative excursions. Protection of the non-conducting light emitting diode from excessive reverse voltage (5 volt maximum allowable) is guaranteed by virtue of the push/pull connection. If only one isolator (rather than two connected in a push/pull configuration) were used per isolator circuit, reverse voltage protection of the light emitting diode, using an ordinary diode, for example, would be required.

Filter capacitors C11 etc. for each isolator circuit cause any incoming noise signals, having frequencies higher than the maximum frequency of interest, to be attenuated.

Because the rate of change of the input voltage at the switching point is not particularly high (certainly at the lowest speed of interest) and because of restrictions on the amount of current drawn from each phase of the generator, the output current (which is approximately proportional to input current) is boosted using emitter followers Q7 etc. When the phase A-B voltage (waveform 6 of Fig. 5) is above about $+1 \cdot 5$ volt the transistor incorporated in the optical isolator Q5 will conduct sufficiently to hold Q7 on, and similarly when the phase A-B voltage is below about $-1 \cdot 5$ volt Q8 will be on. If TP9 is linked to TP8 then the combined outputs from Q7 and Q8 will cause the open collector NAND gate Q3B to switch low for the time the input waveform takes to traverse from the $-1 \cdot 5$ to the $+1 \cdot 5$ volt level (i.e. while neither light emitting diode in Q5 or Q6 conducts). The duration of the Q3B output pulse in the above instance varies from typically about 3% of the repetition period of the generator output at 100% speed to about 6% at 50% speed. Similarly the phase B-C and phase C-A conditioners will cause the outputs of the open collector NAND gates Q3C and Q3D respectively to switch low twice per generator cycle for TP13 linked to TP12 and TP17 linked to TP16. Since the open collector NAND gates Q3B, Q3C and Q3D have their outputs shorted together, six pulses equispaced in time (as shown in the upper waveform 9 of Fig. 5) will be generated at the combined output for each cycle of the three phase tacho-generator output. Note that the switching levels for waveforms 6, 7 and 8 (Fig. 5) have been exaggerated somewhat for illustration purposes.

Susceptibility to input noise is greatest just prior to or just after the normal switching times for the optical isolators. Filter components R37 and C14, and the monostable multivibrator Q4B improve input noise immunity. For the case where 6 pulses are generated at OUTPUT A (upper waveform 10 of Fig. 5) per cycle of the tacho-generator the minimum pulse repetition period is about $2 \cdot 3$ millisecond (corresponding to 105% engine speed). Q4B is connected in the normal retriggerable mode so that, if a noise pulse is received by the multivibrator when its output is true (pulse being generated), the OUTPUT A pulse duration will increase, and in such cases the time interval over which the multivibrator is immune to further noise pulses will be extended. The output pulse duration (waveform 10 of Fig. 5) has been set at $0 \cdot 8$ millisecond which will allow the duration to be increased by more than a factor of 2 (due to retriggering) without causing overlap of consecutive pulses.

Either a positive going or a negative going (from a normally high to a low state) monostable multivibrator output pulse may be taken to OUTPUT A by connecting TP19 to TP18 or TP20 respectively.

To realize the full capability of the frequency to digital converter (to be discussed in Sec. 4.2) it is essential that all pulses received by that converter be counted and the full count be recorded. If, for example, a one second count period were used for the digitization then at 105% engine speed 441 pulses on OUTPUT A would be generated per second. However, for the 8-bit system used at present in the 16 CAD Recorder the maximum count which can be transferred to the recorder is 255 (equal to $2^8 - 1$). Thus 9-bit capacity would be required for complete digitization of the one second count. One way of restricting the digitized output to 8 bits would be to ignore the least significant bit. Although the short term resolution would be unaffected by such a step the long term resolution (counts integrated over a longer time interval) would be affected since each time the counter is reset the least significant bit would be discarded. As indicated in Sec. 3 the ROM in the 16 CAD Recorder has been initially programmed to read engine speed twice per second so that 6 pulses per generator cycle can be handled within the capability of the 8-bit system.

To enable the engine speed input conditioner to be sufficiently versatile for more general purpose use a system of linking via terminal posts TP6 to TP17 has been included to allow operation from single, two or three phase inputs, and to allow selection of the number of pulses generated per cycle of the input (6, 3, 2 or 1 for three phase input; 4, 2 or 1 for two phase input;

2 or 1 for single phase input). Details of the possibilities, according to the terminal post links used, are summarized in the following table.

Number of phases	Number of pulses per cycle	Link connections: Terminal post to be connected to TP9	Link connections: Terminal post to be connected to TP13	Link connections: Terminal post to be connected to TP17	Input connections
3	6	TP8	TP12	TP16	
3	3	TP7	TP11	TP15	As indicated in Fig. 2.
3	2	TP8	TP10	TP14	
3	1	NC*	TP10	TP14	
2	4	TP8	TP12	TP14	Phase 1 to phase A input,
2	2	TP8	TP10	TP14	phase 2 to phase C input,
2	1	NC*	TP10	TP14	common to phase B input
1	2	TP8	TP10	TP14	Between phase A and
1	1	NC*	TP10	TP14	phase B inputs.

* No connection.

If readings of engine speed were to be taken at 1 second intervals (rather than 0·5 second intervals) with the limitations of 8-bit resolution imposed by the present 16 CAD Recorder configuration, then the connection which provides 3 pulses per cycle of the three phase input would be used so that totalizing errors would not occur. Waveforms 9 and 10 (near the bottom of Fig. 5) have been drawn for the case where 3 pulses are generated per cycle of the three phase input.

With the system of linking indicated above, a very versatile conditioner results. For the case where 6 pulses are generated per cycle at the junction of the open collector NAND gates (waveform 9) their duration must be less than $\frac{1}{6}$ (or 17%) of an input signal repetition period to avoid pulse overlap and hence loss of counts. To meet this requirement input signal peak to peak amplitude must be greater than about 6 volt (equal to 2A where Asin30° = 1·5 volt). Basically the circuit will handle a wide range of inputs, sinusoidal or other which are sufficiently high in voltage level and which have sufficient current drive capability for the light emitting diodes in the optical isolators, but input resistor values may have to be altered. Obviously this form of conditioner cannot handle low level signals unless preceded by a suitable pre-amplifier.

As for the fuel flow rate input conditioner the engine speed input conditioner is powered from a single +5 volt supply rail.

4.1.3 Input Address Decoder

The input address decoder comprising devices Q17, Q18 and Q19 (Fig. 2) compares the incoming 4-bit binary address (from the 16 CAD Recorder) with addresses internally set to correspond with the engine speed and fuel flow input addresses, and generates suitable control gates for the frequency to digital converter (Sec. 4.2) when equality occurs.

In the present application the engine speed input has been allocated address 12 (decimal) and the fuel flow input has been allocated address 13. To achieve circuit generality any pair of 4-bit addresses may be nominated via links on TP21 to TP28 and TP29 to TP36 respectively. In this case addresses 12 and 13 have been preset (see dotted connections in Fig. 2). Four bit comparators Q18 and Q19 compare the incoming address with the preselected addresses. Provided the STROBE input to the comparator is low the X and Y outputs will both switch high if the preset and the incoming address are identical.

The incoming command to convert CTC-IN from the 16 CAD Recorder consists of a train of accurately timed (Sec. 3) negative going pulses $\frac{1}{360}$ second (2·78 millisecond) in duration. The CTC-IN signal is inverted via NAND gate Q17B to provide the STROBE control input to comparators Q18 and Q19. The inverted signal designated CTC (Fig. 2) is subsequently used to

initiate conversions in the frequency to digital converter (Sec. 4.2). Low pass filter components R40 and C16 prevent conversions being initiated by any short duration noise spikes received on the CTC-IN input. The CTC-OUT signal is effectively a buffered version of the CTC-IN signal and is taken externally for use with the Digital Signal Monitor (Sec. 3).

In Fig. 6 the address sequence, which has been initially adopted for the engine condition investigations, is indicated over a complete data frame. Waveforms 11, 12, 13 and 14 relating to the address (Fig. 2) illustrate how these inputs change over a data frame. Waveform 15 defines the CTC-IN signal which is characterized by a pulse of $\frac{1}{360}$ second duration generated each time a new address is selected. The negative transition of the CTC-IN coincides with the time of the address advance.

When the CTC-IN is high and address 12 is received the GATE A output (waveform 16) will switch low. The GATE A output controls the engine speed digitizer (Sec. 3) and, as illustrated in Fig. 6, is generated at regular 0·5 second intervals. Similarly GATE B (for the fuel flow digitizer) switches low, but in this case only once per second, when the CTC-IN is high and address 13 is received.

At present digital channels 14 and 15 are not used. By programming the address sequence generated in the 16 CAD Recorder such that channel 14 is addressed twice per second at regular 0·5 second intervals, but displaced 0·25 second with respect to channel 12 address times (refer to Fig. 6), an address decoder which will recognize either address 12 or 14 can be used to enable 4 readings to be taken per second rather than the present 2. Similarly by programming the address sequence such that channel 15 is addressed once per second, but displaced 0·5 second with respect to the time channel 13 is addressed an address decoder which will recognize either address 13 or 15 can be used to enable 2 readings to be taken per second rather than the present 1. These time allocations for addresses 14 and 15 have been included in the initial address sequence (refer to Fig. 6). To obtain the increased sampling rate in each case the normal link between TP37 and TP39 (which sets the engine speed reading rate to twice per second) is removed and that between TP37 and TP38 (relating to fuel flow reading rate) is removed. Removal of the links results in the respective comparator responding to either a "0" or a "1" on the ADDRESS-2 line.

4.2 Frequency To Digital Converter

As indicated in Sec. 3 the frequency to digital converter has been manufactured in the form of a single plug-in board. Complete circuit details are given in Fig. 7 and component layout information is given in Fig. 8. Basically the frequency to digital converter allows two channels of data to be digitized (with up to 12 bit resolution) onto a common output bus.

In the block schema of Fig. 1 the frequency to digital converter has been broken up into functional blocks. The following table lists the identifying labels (Fig. 7) of the integrated circuit devices included in the circuits used to perform the functions indicated in those blocks.

Major block	Minor block	Labels (Fig. 7) of integrated circuit devices used
Digitizer A	Coincidence controlled delay circuit	Q1A, Q5A, Q5B, Q6A, Q6B
	Counter read controller	Q7A, Q7C, Q8A, Q8C
	12-bit counter/latch with tri-state outputs	Q9, Q10, Q11
Digitizer B	Coincidence controlled delay circuit	Q1B, Q5C, Q5D, Q6C, Q6D
	Counter read controller	Q7B, Q7D, Q8B, Q8D
	12-bit counter/latch with tri-state outputs	Q12, Q13, Q14
Read Signal Generator		Q2 (A and B), Q3 (A to D), Q4 (A to F)

Identical circuits are used for digitizer A (which performs a digital conversion on the pulse rate input to INPUT A) and digitizer B. The read signal generator is a common circuit required to control both digitizers. INPUT A and INPUT B are coupled to OUTPUT A (engine speed output) and OUTPUT B (fuel flow rate output) respectively of the input signal conditioner (Fig. 2).

Some indicative pulse polarities and durations for the frequency to digital converter have been shown on the circuit of Fig. 7. Further details on waveforms and their relative timing (as measured on the final circuit) are given in Fig. 9.

Basically the frequency to digital converter provides continuous counting of pulses received on each of its two "pulse rate" inputs (INPUT A and INPUT B), and whenever the A channel (engine speed) or the B channel (fuel flow rate) is addressed via the 16 CAD Recorder, the address decoder (Sec. 4.1.3) causes the GATE A or GATE B output respectively to switch low and the digital output of the corresponding counter to be transferred to the bus. Each time a new data sample is transferred to the bus the following sequence of operations takes place:

(i) Coincidence between the input pulse (INPUT A or INPUT B whichever is applicable) and the read command is checked, and if necessary the counter input is delayed. "Coincidence" is deemed to occur if the negative transition of the input pulse occurs within about 1·2 microsecond after the negative transition of the relevant command to convert (CTC).
(ii) The contents of the counter are transferred to the latch making sure no counter input pulses are received towards the end of the enabling period.
(iii) The counter is reset to the zero count state.
(iv) If coincidence (as per (i)) was detected a delayed input pulse is transferred to the counter.
(v) Counting proceeds normally till another reading is required (0·5 second for engine speed and 1 second for fuel flow rate).
(vi) Overlapping the read interval, during which (i) to (iv) take place, and extending for the remainder of the address period (i.e. while GATE A or GATE B is low, whichever applies) the bus is enabled.

Details on circuit design considerations and on circuit operation follows. Since the operation of digitizer B is identical to that of digitizer A the operation of the latter only will be considered in detail.

INPUT A (waveform 10 of Figs. 5 and 9) is coupled to monostable multivibrator Q1A which generates output pulses of 400 nanosecond (nsec.) nominal duration for each negative transition of INPUT A. Both positive going and negative going multivibrator output pulses are produced, where the negative going pulse output is defined (Fig. 7) as V_{1A} (waveform 18 of Fig. 9). AC coupling at the multivibrator output causes 200 nsec. nominal duration pulses to be generated at the leading and trailing edges of the multivibrator output. These pulses, V_{2A} and V_{3A} (Fig. 7) respectively, form separate outputs.

V_{2A} may be considered to be a "prepulse" train and V_{3A} a "counter input" pulse train. When enabled by GATE A (waveform 16 of Fig. 6) the V_{2A} pulse train is transferred to the output of AND gate Q8C for which waveform 19 of Fig. 9 applies. V_{2A} is compared with the CTC input (waveform 21 of Fig. 9) for coincidence. If coincidence is not detected the following V_{3A} pulse will be coupled via gates Q6A and Q5A to the counter input (upper waveform 20 of Fig. 9). If coincidence is detected the V_{3A} pulse will be temporarily delayed (lower waveform 20 of Fig. 9) until the counter latch/clear sequence has terminated. Details on how the performance, indicated in this paragraph, is achieved will be given subsequently.

The choice of 200 nsec. for the V_{2A} and V_{3A} pulse durations is fairly arbitrary; such durations could have been made shorter or longer. However such durations are long enough to enable "full" amplitude pulses to be generated after the AC coupling capacitors (C4 and C5) and to enable fairly convenient viewing with a monitoring oscilloscope (used during development), but are not so long that the slower trailing edge transitions could give rise to multiple pulse generation or that the range of input frequencies which may be accommodated is unnecessarily reduced. The nominal separation between the trailing edge of the V_{2A} pulse and the leading edge of the V_{3A} pulse is 200 nsec. This interval has to be sufficiently long to allow detection of the pre-pulse V_{2A} by the coincidence check circuits and the generation of a suitable gate signal to prevent the transfer of the following V_{3A} pulse to the A counter. The 200 nsec. interval easily accommodates all the inherent circuit propagation delays.

Each time a negative transition occurs on the CTC input an 800 nsec. nominal duration LATCH pulse (waveform 22 of Fig. 9) is generated at the 1Q output of monostable multivibrator Q2A. When the LATCH pulse is high the count state in the binary counter/latches (Q9 to Q11 for A and Q12 to Q14 for B) is transferred to the latches. The latches retain the count state present at the time the LATCH pulse switches back low. The counters count normally during the latch sequence if count pulses are received. Latching in both A and B counters will take place for each address advance but the tri-state outputs will not be enabled except when the relevant addresses are decoded.

Reasons for the choice of 800 nsec. duration for the LATCH pulse will now be examined. If the trailing edge of a V_{2A} pulse coincides with the leading edge of the LATCH pulse (or more correctly the CTC input transition which causes that transition of the LATCH pulse) it will probably just miss being detected by the coincidence circuit so that, in that case, a normal V_{3A} pulse will be transferred to the counter nominally 200 nsec. later (let us say 300 nsec. to allow a margin). The maximum propagation delay through a single stage DM8554 counter (Fig. 7) is stated by the manufacturers to be 70 nsec. A multistage mode of connection which will reduce delays, for up to 7 cascaded stages[4], to that equivalent to a 2-stage counter is used. Thus at least 140 nsec. propagation delay should be allowed for (let us allow 250 nsec. which will also accommodate the alternative straight "ripple through" connection of the 3-stage counter). Thus with 800 nsec. LATCH pulse duration there is an interval of at least 250 nsec. duration at the latter end of the LATCH pulse for which the state of the counter is guaranteed not to change.

The GATE A input from the address decoder is taken to the A-BUS ENABLE (Fig. 7) input of the binary counter/latches Q9 to Q11. At the time of the negative excursion of the CTC input the GATE A input switches low and remains low for the remainder of the relevant address period (i.e. until the next CTC switches high). The A-BUS ENABLE pulse overlaps the LATCH pulse but this is quite acceptable provided the bus is not interrogated by the 16 CAD Recorder until after the LATCH pulse has terminated.

For the present sampling arrangement as indicated in Fig. 6 (assuming addresses 12 and 13 correspond to the A and B inputs respectively) the duration of the A-BUS ENABLE (i.e. time for which GATE A is low) is $\frac{17}{360}$ second (47·2 millisecond approximately).

At the end of the LATCH period (800 nsec. nominal duration) a short duration (100 nsec. nominal) pulse V_{1R} (waveform 23 of Fig. 9) is generated at the input to the monostable multivibrator Q2B. The duration of this pulse is set by the values of the coupling components C9 and R9, and provides adequate separation between LATCH and counter clear (CR) pulses. Starting at the trailing edge of this short duration pulse the monostable multivibrator Q2B generates a pulse V_{3R} (waveform 26 of Fig. 9) of 600 nsec. nominal duration. On the leading edge of this multivibrator output pulse coupling components C13 and R13 generate a positive going pulse (of 200 nsec. duration nominally) which is buffered via inverters Q4E and Q4D to give the CR output (waveform 24 of Fig. 9) and steered via AND gates Q8A and Q8B to either counter A (comprising Q9 to Q11) or counter B (comprising Q12 to Q14) under the control of the GATE A and GATE B inputs. The 200 nsec. duration pulses generated at the outputs of Q8A and Q8B respectively constitute the clear pulses (CR-A and CR-B respectively). Once again the 200 nsec. duration is fairly arbitrary but the same considerations as for the generation of the V_{2A} and V_{3A} pulses apply. The clear pulses reset the respective counters to the zero count condition.

"Coincidence" between an input pulse and the CTC received at the time the appropriate address is decoded is checked with the aid of a COINCIDENCE TEST GATE V_{2R} (waveform 25 of Fig. 9). This test gate in effect encompasses a time interval which includes a LATCH pulse and a subsequent CR pulse. The test gate is of fixed duration (nominally 1·1 microsecond) and is generated for each CTC pulse received. It starts nominally at the time the CTC switches low and terminates at the trailing edge of the CR pulse (output of Q4D). The test gate is generated at the output of NAND gate Q3B which, together with Q3A, forms a flip flop which is nominally set when the Q output of the monostable multivibrator Q2A switches low (i.e. the time the CTC switches low if propagation delays are ignored) and cleared at the trailing edge of the CR pulse. The reset pulse for the flip flop is derived from Q4D via Q4C, AC coupling components C8 and R8, and inverter Q4A. The coincidence test gate is generated for each CTC pulse received. The test gate has been arranged to terminate at the trailing edge of the CR pulse as clock pulses must be prevented from reaching the counters during the LATCH (latter portion) and CLEAR sequences.

When GATE A and the COINCIDENCE TEST GATE are both in their "true" states ("low" and "high" respectively) and a prepulse V_{2A} is received, the output of the open collector NAND gate Q7C will switch low causing the output V_{4R} (waveform 27 of Fig. 9) of the "INHIBIT GATE" flip flop (comprising NAND gates Q3C and Q3D) to switch low. Similarly V_{4R} will switch low if a V_{2B} prepulse is received when GATE B is low and the COINCIDENCE TEST GATE is high. Open collector NAND gates Q7C and Q7D provide a low state "wire-OR" function. In this application Q7C and Q7D are never activated at the same time. The INHIBIT GATE V_{4R} can switch low only when the COINCIDENCE TEST GATE is high. At the trailing edge of the V_{3R} pulse (waveform 26 of Fig. 9) generated by monostable multivibrator Q2B a reset pulse is transferred to the INHIBIT GATE flip flop. If the flip flop has been set the INHIBIT GATE V_{4R} will switch back from low to high; if it has not been set, no change in the flip flop state will occur.

The INHIBIT GATE signal is steered under the control of the GATE A or GATE B inputs to either the A or the B digitizers using OR gates Q5B or Q5C respectively. If a V_{3A} (Fig. 7) counter input pulse arrives when the INHIBIT GATE is low transfer of the V_{3A} pulse via AND gate Q6A will be inhibited.

Using buffer Q6B, AC coupling components C11 and R11, and OR gate Q5A, a positive going pulse (waveform 20 at bottom of Fig. 9) of 200 nsec. nominal duration will be transferred to the A counter input at the time the INHIBIT GATE switches back high (which will, of course, occur only if "coincidence" has been detected). Thus, in effect, a delayed counter input pulse is transferred to the A counter. Gating of pulses to the B counter follows exactly the same logic.

With the timing arrangement described, the INHIBIT GATE may have a duration anywhere between about 350 nsec. (minimum) and 1,500 nsec. (maximum) as indicated in waveform 27 of Fig. 9. The leading edge always coincides nominally with a V_{2A} or V_{2B} prepulse leading edge and hence non-coincidence with the V_{3A} or V_{3B} pulse respectively is guaranteed.

If the leading edge of a V_{2A} prepulse is just detected at the trailing edge of the COINCIDENCE TEST GATE then the INHIBIT GATE V_{4R} must continue to remain low for a period which guarantees that the delayed counter input pulse is transferred later than or overlaps the V_{3A} pulse which follows the V_{2A} prepulse. If either of these conditions is satisfied the transfer of only one pulse to the counter is guaranteed. Thus the INHIBIT GATE must remain low for at least 200 nsec. after the trailing edge of the COINCIDENCE TEST GATE. To allow a margin, the minimum time has been made 350 nsec. approximately as mentioned above. This interval is set by the difference between the monostable multivibrator Q2B output pulse duration (560 nsec. measured value as indicated in Fig. 9) and the CR pulse duration (210 nsec. measured value).

The maximum time that a V_{3A} pulse can be delayed (because of the coincidence check and the inhibit routine) is nominally the maximum interval between the negative transition of the CTC and the trailing edge of the INHIBIT GATE (measured value 1,560 nsec. as indicated in waveform 20 at bottom of Fig. 9) less the interval between the trailing edge of a V_{2A} prepulse and the leading edge of the following V_{3A} pulse (200 nsec. measured value). Thus the maximum delay of the counter input pulse is about 1·4 microsecond (as indicated by τ_D (max.) of Fig. 9).

Measurements on the final unit indicated that input signals (to INPUT A or INPUT B) with rates up to 700 KHz can be handled. The minimum time interval between successive frequency to digital conversions, which can be handled, is the repetition period of the 700 KHz signal (1·4 microsecond approximately). Thus for regular conversions of N digital channel inputs, each sampled at the same rate, the maximum conversion rate for each channel will be given by

$$\frac{700}{N} \text{ KHz.}$$

As indicated in Sec. 4.1.2 it is essential that all pulses received by the frequency to digital converter be counted, and the full count be transferred to the output bus, if accurate totalizing is a requirement. However in some instances accurate totalizing may not be a requirement. In such cases counter bits of lowest significance may be ignored to allow higher input frequencies to be handled but only when the capacity of the acquisition system is less than 12 bits. For this reason a set of terminal posts X0 to X11 for the A counter outputs, Y0 to Y11 for the B counter outputs and Z0 to Z11 for the outputs to the bus may be suitably linked to couple the desired outputs, individually selected for the A and B counters, to the bus. When accurate totalization is required the least significant bit must be transferred to the bus. For the 8-bit recording system to be used for studies on the Viper engine the link connections given in the following table have been adopted.

Output line (connected to bus)	Internal links (Figs. 7 & 8) to that line
B0	Z0 → Y4 → X4
B1	Z1 → Y5 → X5
B2	Z2 → Y6 → X6
B3	Z3 → Y7 → X7
B4	Z4 → Y8 → X8
B5	Z5 → Y9 → X9
B6	Z6 → Y10 → X10
B7	Z7 → Y11 → X11
B8	Z8 → Y0 → X0*
B9	Z9 → Y1 → X1*
B10	Z10 → N.C.
B11	Z11 → N.C.

N.C. = No connection

* This linking effectively produces zeros on the B8 and B9 output lines when either engine speed or fuel flow rate outputs are interrogated but leaves these lines free to change when the ADC (10-bit capacity but two least significant bits not processed) in the 16 CAD Recorder is interrogated.

As indicated in Fig. 7 LATCH, CR and TEST GATE outputs (which control both the A and the B digitizers) are taken to edge connector pins. In the present application these outputs are not used. For added versatility these outputs have been made available for systems in which a larger number of pulse rate inputs are to be digitized. In such cases the complete read signal generator (incorporating Q2, Q3, Q4 and associated components) need not be repeated.

4.3 Power Supply

In line with one of the primary objectives of the conditioner development the power supply has been made quite simple. All conditioner circuits require only a single +5 volt supply.

The +5 volt supply is derived from the aircraft 28 volt DC supply via a DC to DC converter power supply PS1 (listed under "Components For Mainframe" in Appendix I). Isolation of the output circuit common from aircraft ground is thereby achieved. Wiring information on the PS1 power supply is given in Appendix III.

In the following table the supply current requirements for the various circuits are listed.

Circuit detail		Current demand from +5 volt supply	
Input signal conditioner	(i) Fuel flow and engine speed input conditioners	(i) 50 mA (milliamp)	120 mA
	(ii) Input address decoder	(ii) 70 mA	
Frequency to digital converter			520 mA
	Total		640 mA

Further as indicated in Fig. 1 +5 volt is taken externally to power the Digital Signal Monitor which typically draws about 380 mA. Hence the total current demand from the +5 V supply is 1,020 mA.

Regulation of the PS1 supply is not particularly good, but is satisfactory for this fairly non-critical application. Some details on the variation in "regulated" output voltage with output current, for the particular unit used, are given in the following table.

Voltage output of DC to DC converter power supply PS1	5·90	5·39	5·29	5·18	4·94	4·80	4·60
Current (mA) drawn from +5 volt supply	0	50	100	200	400	800	1,350

When the Digital Signal Monitor is plugged in (only occurs during pre-flight checks) the output voltage typically drops by about 0·11 volt.

The current drawn from the aircraft 28 volt DC supply is 340 mA for the complete conditioning equipment without the Digital Signal Monitor connected, and increases to 475 mA with the Monitor connected.

5. DETAILS ON THE COMPLETED CONDITIONER

The conditioning equipment comprising all the circuits detailed in Sec. 4 has been manufactured as a unit bearing the name "Engine Speed And Fuel Flow Rate Digitizer". A photograph of the completed unit is given in Fig. 10 and photographs of the Input Signal Conditioner printed circuit assembly and the Frequency to Digital Converter printed circuit assembly are given in Figs. 11 (a) and 11 (b) respectively.

External connection to the Digitizer is made via five connectors according to the following table.

Connector identification	Destination
6J1	28 volt DC power input
6J2	Fuel flow rate input
6J3	Engine speed input
6J4	Digital output to and control input from 16 CAD Recorder
6J5	Digital output to Digital Signal Monitor

Details of internal wiring to these connectors and also to the printed circuit edge connectors 6J6 and 6J7 are given in Appendix III.

Satisfactory performance of the Digitizer has been demonstrated over the temperature range −20 to +60 degrees Celsius (performance outside that range has not been checked). The maximum input pulse rate which can be handled by the Frequency to Digital Converter without loss of any counts during read sequences was found to be in excess of 700 KHz throughout the above temperature range.

It is to be noted that generally type SN7400 digital integrated circuits have been used. Although performance of these circuits over the temperature range 0 to 70 degrees Celsius only is guaranteed, satisfactory operation outside these limits is possible. All the integrated circuits used, which have the 0 to 70 degrees specified range of temperature for satisfactory operation, can be replaced directly with types (SN5400 in place of SN7400 for instance) having performance guaranteed over the range −55 to +125 degrees Celsius.

Recently the Digitizer was installed in the nosebay of a Macchi aircraft where it forms part of the equipment to be used for Viper engine condition evaluation studies. It has performed satisfactorily during flight tests which have been undertaken so far.

CONCLUSION

The conditioner described converts quantities sensed as analogue frequencies to digital form. It has the following salient characteristics:

(a) The binary converter has 12-bit capacity providing a maximum resolution of 1 part in 4,096 of full scale per reading.

(b) Signal frequencies up to 700 KHz can be handled without any counts being missed when the data are read but restrictions relating to counter overflow need to be observed.

(c) Digitization may be performed at rates up to $\frac{700}{N}$ KHz where N is the number of separate frequency signals to be digitized.

(d) No counts are missed as the frequency signals are digitized so that very accurate totalizing (of engine revolutions or fuel consumed for instance) is made possible by adding successive contributions. Improved resolution is achieved if the readings are summed over a longer time interval but the ability to follow rapid changes in the quantity being sensed will be reduced proportionately.

REFERENCES

1. M. T. Adams — Digital Data Acquisition System For Aircraft Engine Condition Monitoring. To be published.
2. K. F. Fraser, and U. R. Krieser — Airborne Data Processor. To be published.
3. B. Drazenovic — Digital Signal Monitor. A.R.L./M.E. Tech. Memo 365
4. National Semiconductor Digital Data Handbook. June 1973, page 1.155.

Appendix I

COMPONENT LISTS

The following tables list the components used in the circuits described in the text. Components used in these circuits have been given an identification label (or legend) consisting of a letter prefix followed by a number. The letter prefix identifies the class of component as indicated in the following table.

Class of component	Letter prefix
Resistor	R
Capacitor	C
Diode	CR
Inductor	L
Transistor or Integrated Circuit	Q
Terminal Post	TP
Test Socket	TS
Power Supply	PS
Chassis Mounted Connector	J

The number following the letter prefix identifies the particular component of the specified class.

Resistance, capacitance and inductance values given in the component lists (and also marked on the circuit diagrams) are given respectively in unit of ohm, picofarad and microhenry (where K = 10^3 and M = 10^6 multiplication factors). Thus a capacitance value designated 10K means 10,000 picofarad and a capacitance value designated 6·8M means $6{\cdot}8.10^6$ picofarad or 6·8 microfarad.

Components for input signal conditioner

Legend	Value	Description
R1	2·2K	Resistor, fixed, glass-tin-oxide, style RFG5, Electrosil
R2	10	Resistor, fixed, carbon, CR68, Philips (value to be selected)
R3	2·2K	As for R1
R4 (A & B)	47K	As for R1 (space for two resistors in parallel), match with R5 to 0·5%
R5 (A & B)	47K	As for R1 (space for two resistors in parallel), match with R4 to 0·5%
R6	10K	As for R1
R7	10K	As for R1
R8	4·7K	As for R1
R9	10	As for R1
R10	10K	As for R1
R11	47K	As for R1
R12	47K	As for R1
R13	4·7K	As for R1
R14	4·7K	As for R1
R15	4·7K	As for R1
R16	4·7K	As for R1
R17	4·7K	As for R1
R18	27K	As for R1

Legend	Value	Description
R19	1·8K	As for R1
R20	1·5K	As for R1
R21	4·7K	As for R1
R22	4·7K	As for R1
R23	4·7K	As for R1
R24	4·7K	As for R1
R25	1·8K	As for R1
R26	1·5K	As for R1
R27	4·7K	As for R1
R28	4·7K	As for R1
R29	4·7K	As for R1
R30	4·7K	As for R1
R31	1·8K	As for R1
R32	1·5K	As for R1
R33	4·7K	As for R1
R34	4·7K	As for R1
R35	4·7K	As for R1
R36	4·7K	As for R1
R37	100	As for R1
R38	2·2K	As for R1
R39	10K	As for R1
R40	100	As for R1
C1	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D, 35 VW
C2	6·8M	As for C1
C3	100K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 104K
C4	100K	As for C3
C5	47M	Capacitor, fixed, electrolytic, tantalum, ITT, TAG, 6·3VW
C6	10K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 103K
C7	680	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 681K
C8	10K	As for C6
C9	10K	As for C6
C10	1M	Capacitor, fixed, electrolytic, tantalum, Sprague type CS13
C11	470K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 474K
C12	470K	As for C11
C13	470K	As for C11
C14	470K	As for C11
C15	330K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 334K
C16	100	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 101K
C17	6·8M	As for C1
C18 → C22	10K	As for C6
L1	27	Inductor, fixed, Cambion type 2590/30
Q1		Integrated circuit, voltage comparator, National Semiconductor, LM311D
Q2		As for Q1
Q3		Integrated circuit, quad 2-input NAND gate, open collector, SN7403N
Q4		Integrated circuit, dual retriggerable monostable multivibrator, SN74123N
Q5		Integrated circuit, optically coupled isolator, Hewlett Packard type 5082-4350
Q6		As for Q5
Q7		Transistor, silicon, NPN, SE4010

Legend	Value	Description
Q8		As for Q7
Q9		As for Q5
Q10		As for Q5
Q11		As for Q7
Q12		As for Q7
Q13		As for Q5
Q14		As for Q5
Q15		As for Q7
Q16		As for Q7
Q17		Integrated circuit, quad 2-input AND gate, SN7408N
Q18		Integrated circuit, 4-bit digital comparator, National Semiconductor, DM8200
Q19		As for Q18
CR1 → CR3		Diode, silicon, OA202
TP1 → TP36		Terminal post, Cambion, type 2081-1

Components for frequency to digital converter

Legend	Value	Description
R1	9·1K	Resistor, fixed, glass-tin-oxide, style RFG5, Electrosil
R2	8·2K	As for R1
R3	9·1K	As for R1
R4 → R9	470	As for R1
R10	10K	As for R1
R11 → R14	470	As for R1
R15 → R17	1·2K	As for R1
C1	120	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 121K
C2	270	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 271K
C3	120	As for C1
C4	330	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 331K
C5	330	As for C4
C6	330	As for C4
C7	330	As for C4
C8	330	As for C4
C9	220	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 221K
C10	180	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 181K
C11	330	As for C4
C12	330	As for C4
C13	330	As for C4
C14	330	As for C4
C15	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D, 35VW
C16 → C29	10K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW 103K
L1	27	Inductor, fixed, Cambion type 2590/30
Q1		Integrated circuit, dual retriggerable monostable multivibrator, SN74123N
Q2		As for Q1
Q3		Integrated circuit, quad 2-input NAND gate, SN7400N
Q4		Integrated circuit, hex inverter, SN7404N
Q5		Integrated circuit, quad 2-input OR gate, SN7432N
Q6		Integrated circuit, quad 2-input AND gate, SN7408N
Q7		Integrated circuit, quad 2-input NAND gate with open collector, SN7403N
Q8		As for Q6
Q9 → Q14		Integrated circuit, 4-bit binary counter/latch/tri-state output, DM8554
TP1 → TP36		Terminal post, Cambion, type 2081-1
TS1		Test socket, red, Amp Part No. 3-582118-2
TS2		Test socket, yellow, Amp Part No. 3-582118-4
TS3		Test socket, green, Amp Part No. 3-582118-5
TS4		Test socket, white, Amp Part No. 3-582118-9
TS5		Test socket, blue, Amp Part No. 3-582118-6
TS6		As for TS2
TS7		As for TS3
TS8		As for TS5
TS9		As for TS2
TS10		As for TS3
TS11		Test socket, black, Amp Part No. 3-582118-0

Components for mainframe

Legend	Description
PS1	DC to DC Converter Power Supply, Tecnetics Model 9586-102, 28V input, 5V (regulated) output, 10 watt (i.e. 2 amp) rated output
6J1	Plug, chassis mounted, Cannon KPT02E8-4P
6J2	Plug, chassis mounted, Cannon KPT02E8-3P
6J3	Plug, chassis mounted, Cannon KPT02E10-6P
6J4	Plug, chassis mounted, Cannon KPT02E14-19P
6J5	Socket, chassis mounted, Cannon KPT02E14-19S
6J6	Printed circuit edge connector, double sided, 28 contacts per side, Cannon GO D56 B2AAKG
6J7	As for 6J6

Appendix II

DIGITAL INTEGRATED CIRCUIT SUPPLY CONNECTIONS

Supply connections, some of which are not indicated on the circuit, are given in the following table.

Circuit card	Device identification		Connected to Vcc	Connected to Com	Package* size
	Legend	Type			
Input signal conditioner	Q3	SN7403N	14	7	14DIL
	Q4	SN74123N	16	8	16DIL
	Q17	SN7400N	14	7	14DIL
	Q18	DM8200N	14	7	14DIL
	Q19	DM8200N	14	7	14DIL
Frequency to digital converter	Q1	SN74123N	16	8	16DIL
	Q2	SN74123N	16	8	16DIL
	Q3	SN7400N	14	7	14DIL
	Q4	SN7404N	14	7	14DIL
	Q5	SN7432N	14	7	14DIL
	Q6	SN7408N	14	7	14DIL
	Q7	SN7403N	14	7	14DIL
	Q8	SN7408N	14	7	14DIL
	Q9	DM8554	16, 9, 10	8, 13	16DIL
	Q10	DM8554	16, 9	8, 13	16DIL
	Q11	DM8554	16	8, 13	16DIL
	Q12	DM8554	16, 9, 10	8, 13	16DIL
	Q13	DM8554	16, 9	8, 13	16DIL
	Q14	DM8554	16	8, 13	16DIL

* DIL means dual-in-line package.

All digital integrated circuits are mounted with a 10,000 picofarad power supply bypass capacitor in close proximity to the device.

Appendix III

INTERWIRING DETAILS

Details of all interwiring within the signal conditioning unit are given in this Appendix. The types of cable specified in the following table are used for the interwiring.

Legend	Description
W1	Cable, twisted pair (black and white insulation respectively), shielded, Raychem type 44A1121-9/0-9
W2	Cable, co-axial, 125 ohm impedance, Raychem type 44A1111-26-9-9
W3	Cable, single core, multi-stranded, grey insulation, Raychem type 44A0111-28-8
W4	Cable, single core, multi-stranded, Ascand 7/0·010, black PVC insulation
W5	Cable, single core, multi-stranded, Ascand 7/0·010, red PVC insulation

A summary of the connectors together with their application is given in the following table. Details on the types of connectors (referred to in this Appendix) are given in Appendix I.

Connector	Location	Application
6J1	Rear panel	Aircraft input power connector
6J2	Rear panel	Fuel flow signal input connector
6J3	Rear panel	Engine speed signal input connector
6J4	Rear panel	Input/output connector for recording equipment
6J5	Rear panel	Output connector for display equipment
6J6	Internal chassis	Printed circuit edge connector for Input Signal Conditioner—Board 1
6J7	Internal chassis	Printed circuit edge connector for Frequency to Digital Converter—Board 2

(a) *Wiring to 6J1 (power input)*

Pin	Connected to	Signal Description	Wire type
A	PS1 → +input	+28V input (aircraft power)	W5
B	PS1 → −input	28V return (power input ground)	W4
C	Chassis lug	Case ground	W4
D	Chassis lug	External cable shield	W4

(b) *Wiring to 6J2 (fuel flow input)*

Pin	Connected to	Signal description	Wire type
A	6J6—27	Fuel flow signal input	W1—white
B	6J6—EE	Fuel flow signal common (connected externally to aircraft frame)	W1—black
C	Left open at the input to 6J6	Cable shield	W1—shield

(c) *Wiring to 6J3 (engine speed input)*

Pin	Connected to	Signal description	Wire type
A	6J6—8	Phase A input from tacho. gen.	W2—inner
B	Left open at the input to 6J6	Shield for phase A	W2—shield
C	6J6—7	Phase B input from tacho. gen.	W2—inner
D	Left open at the input to 6J6	Shield for phase B	W2—shield
E	6J6—7	Phase C input from tacho. gen.	W2—inner
F	Left open at the input to 6J6	Shield for phase C	W2—shield

(d) *Wiring to 6J4 (recorder input/output)*

Pin	Connected to	Signal description	Wire type
A	6J5—A	BIT 0 (MSB)	W3
B	6J5—B	BIT 1	W3
C	6J5—C	BIT 2	W3
D	6J5—D	BIT 3	W3
E	6J5—E	BIT 4	W3
F	6J5—F	BIT 5	W3
G	6J5—G	BIT 6	W3
H	6J5—H	BIT 7	W3
J	6J5—J	BIT 8	W3
K	6J5—K	BIT 9	W3
L	6J5—L	BIT 10	W3
M	6J7—2	COM	W4
N	6J6—26	CTC	W2—inner*
P	6J5—P	BIT 11	W3
R	6J5—R	ADDRESS 8	W3
S	6J5—S	ADDRESS 4	W3
T	6J5—T	ADDRESS 2	W3
U			
V	6J5—V	ADDRESS 1	W3

* Shield connected to 6J4—M at one end and left open at the other.

(e) *Wiring to 6J5 (display output)*

Pin	Connected to	Signal description	Wire type
A	6J4—A, 6J7—27	BIT 0 (MSB)	W3
B	6J4—B, 6J7—26	BIT 1	W3
C	6J4—C, 6J7—25	BIT 2	W3
D	6J4—D, 6J7—23	BIT 3	W3
E	6J4—E, 6J7—21	BIT 4	W3
F	6J4—F, 6J7—18	BIT 5	W3
G	6J4—G, 6J7—17	BIT 6	W3
H	6J4—H, 6J7—15	BIT 7	W3
J	6J4—J, 6J7—13	BIT 8	W3
K	6J4—K, 6J7—11	BIT 9	W3
L	6J4—L, 6J7—8	BIT 10	W3
M	6J7—B	COM	W4
N	6J6—20	CTC	W2—inner*
P	6J4—P, 6J7—6	BIT 11	W3
R	6J4—R, 6J6—25	ADDRESS 8	W3
S	6J4—S, 6J6—DD	ADDRESS 4	W3
T	6J4—T, 6J6—23	ADDRESS 2	W3
U	PS1 (+output)	+5V POWER	W5
V	6J4—V, 6J6—24	ADDRESS 1	W3

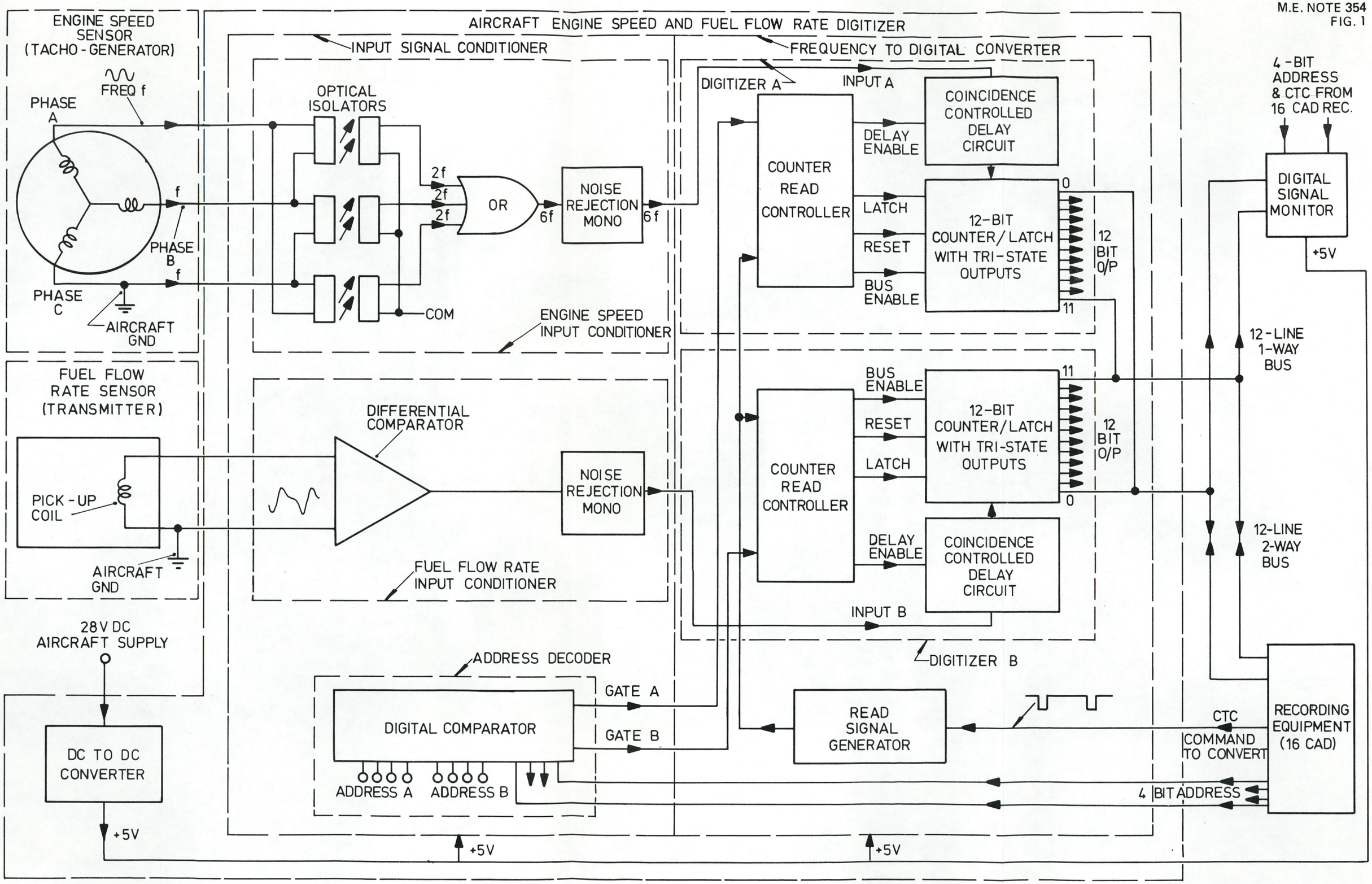
* Shield connected to 6J5—M at one end and left open at the other.

(f) *Wiring to 6J6 (input signal conditioner edge connector)*

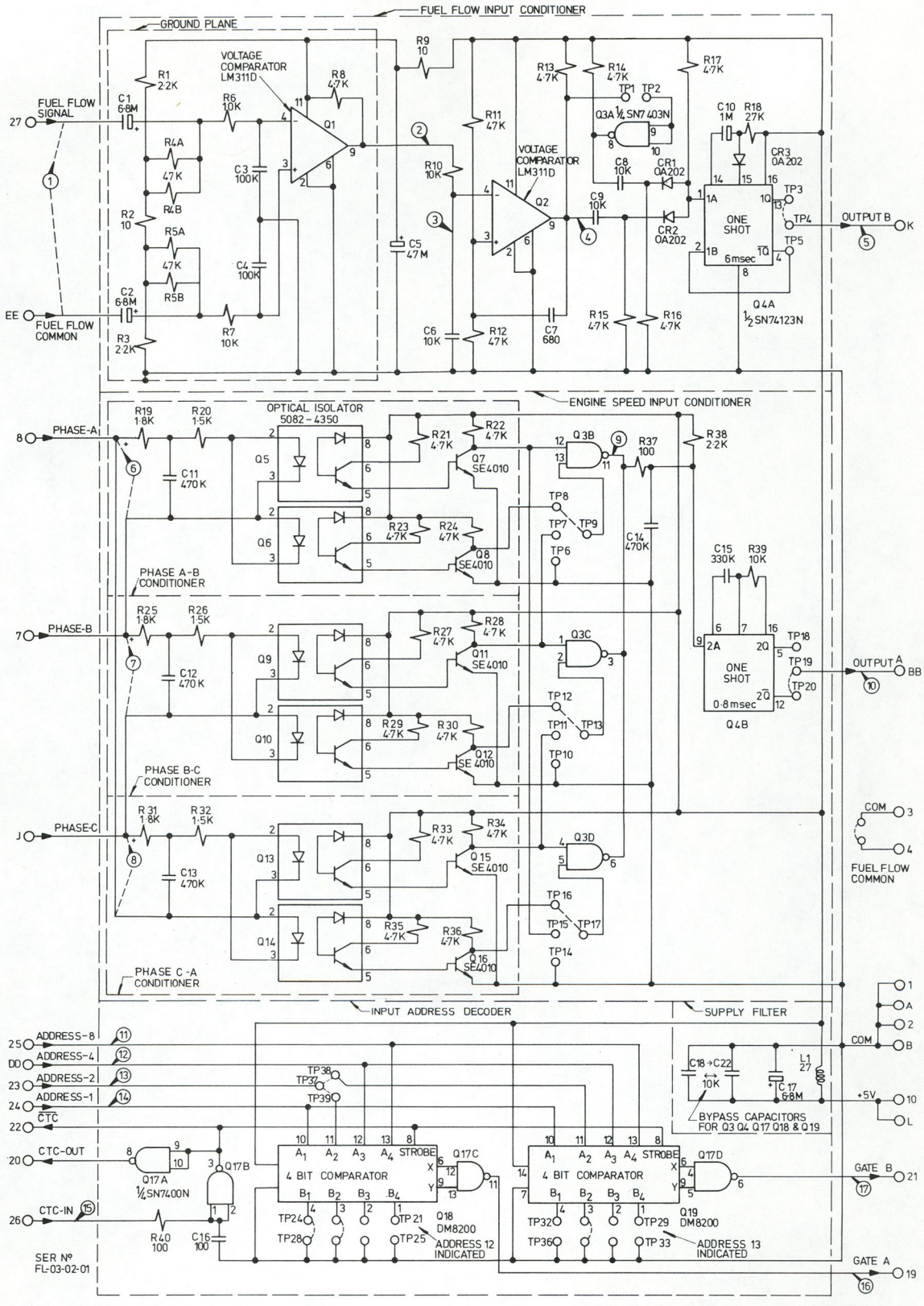
Pin	Connected to	Pin	Connected to
1	6J6—A, 6J6—2	A	6J7—1, 6J6—B, 6J6—1
2	6J6—1, 6J6—B	B	6J7—A, 6J6—2
3	6J6—2	C	
4	6J6—EE	D	
5		E	
6		F	
7	6J3—C	H	
8	6J3—A	J	6J3—E
9		K	6J7—R
10	6J6—L	L	6J7—10, 6J6—10
11		M	
12		N	
13		P	
14		R	
15		S	
16		T	
17		U	
18		V	
19	6J7—E	W	
20	6J5—N	X	
21	6J7—J	Y	
22	6J7—28	Z	
23	6J5—T	AA	
24	6J5—V	BB	6J7—4
25	6J5—R	CC	
26	6J4—N	DD	6J5—S
27	6J2—A	EE	6J2—B
28		FF	

(g) *Wiring to 6J7 (frequency to digital converter edge connector)*

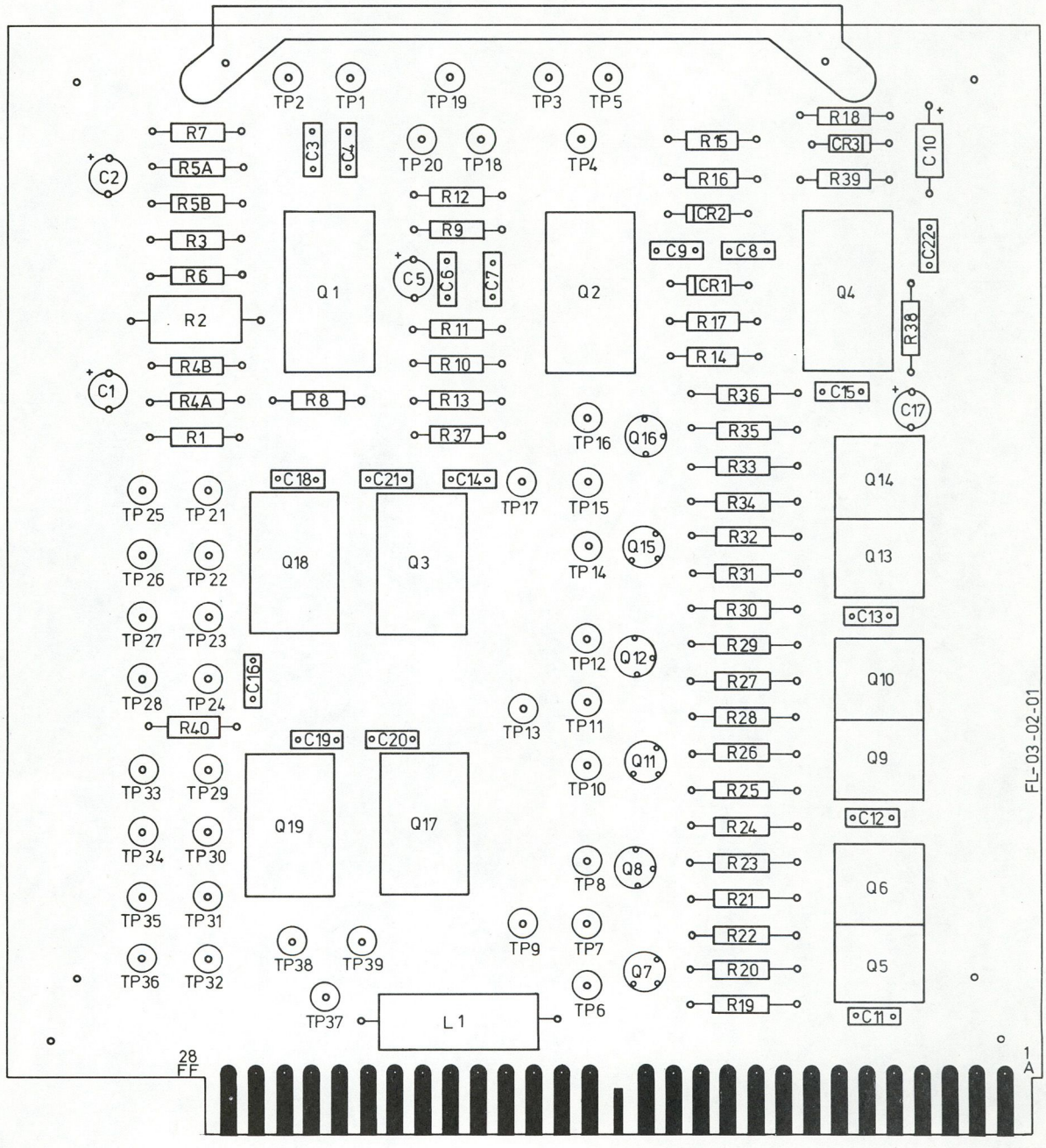
Pin	Connected to	Pin	Connected to
1	6J7—A, 6J7—2, 6J6—A	A	PS1 (—output), 6J7—B, 6J7—1
2	6J7—B, 6J7—1, 6J4—M	B	6J7—A, 6J7—2, 6J5—M
3		C	
4	6J6—BB	D	
5		E	6J6—19
6	6J5—P	F	
7		H	
8	6J5—L	J	6J6—21
9		K	
10	6J7—L, 6J6—L	L	PS1 (+ output), 6J7—10
11	6J5—K	M	
12		N	
13	6J5—J	P	
14		R	6J6—K
15	6J5—H	S	
16		T	
17	6J5—G	U	
18	6J5—F	V	
19		W	
20		X	
21	6J5—E	Y	
22		Z	
23	6J5—D	AA	
24		BB	
25	6J5—C	CC	
26	6J5—B	DD	
27	6J5—A	EE	
28	6J6—22	FF	



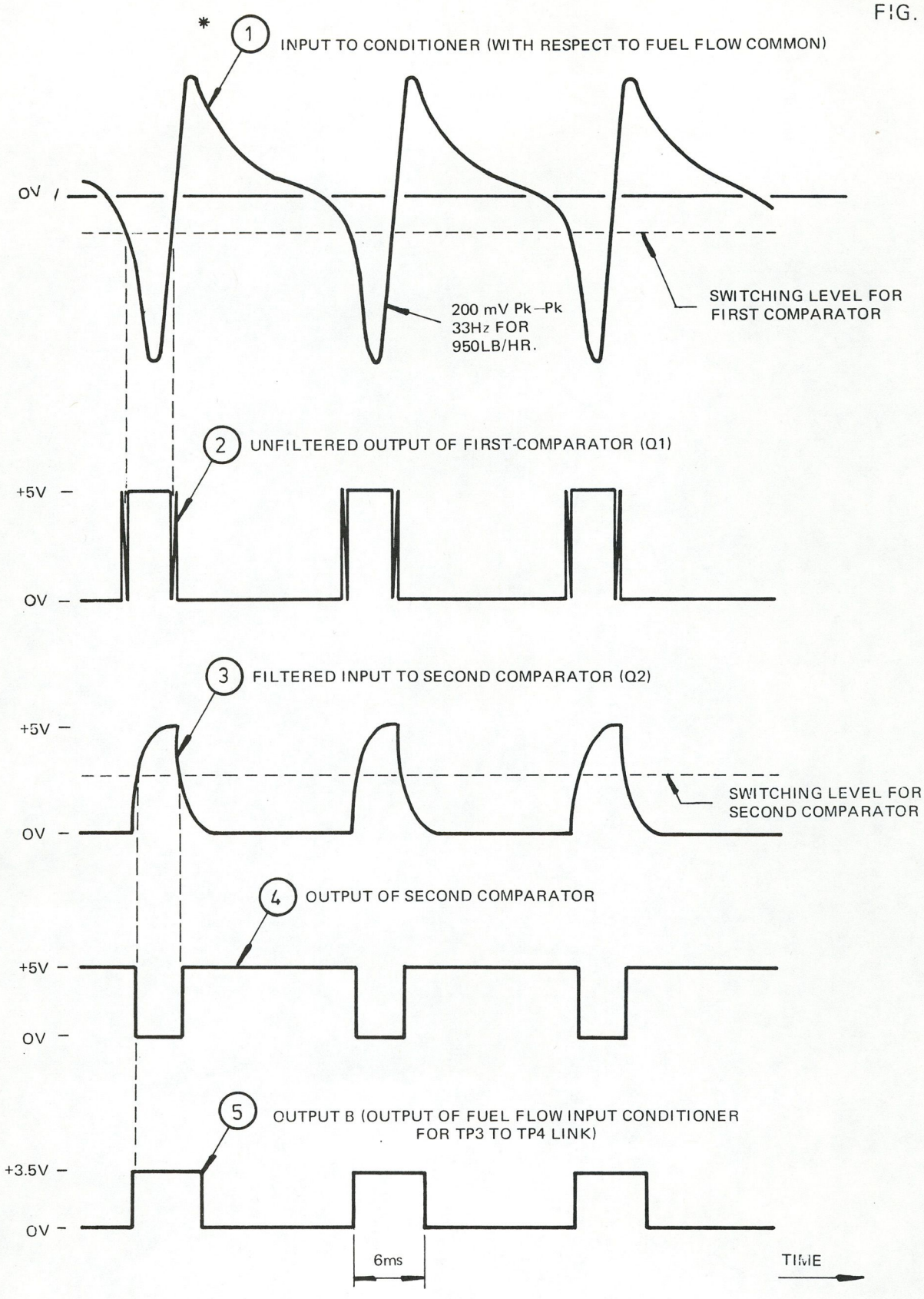
BLOCK SCHEMA OF SYSTEM OF DIGITIZATION FOR ENGINE SPEED AND FUEL FLOW RATE



INPUT SIGNAL CONDITIONER

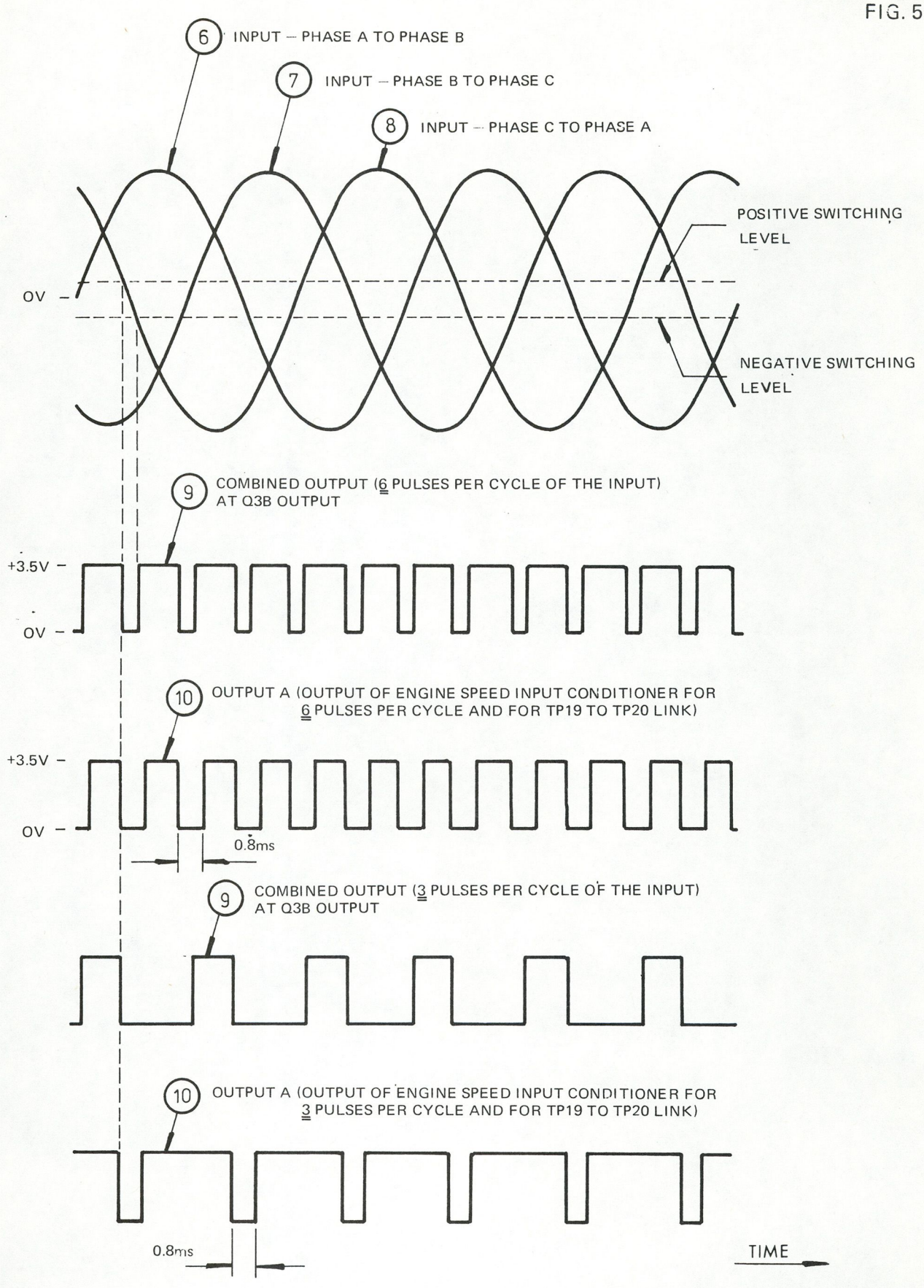


COMPONENT LAYOUT FOR INPUT SIGNAL CONDITIONER

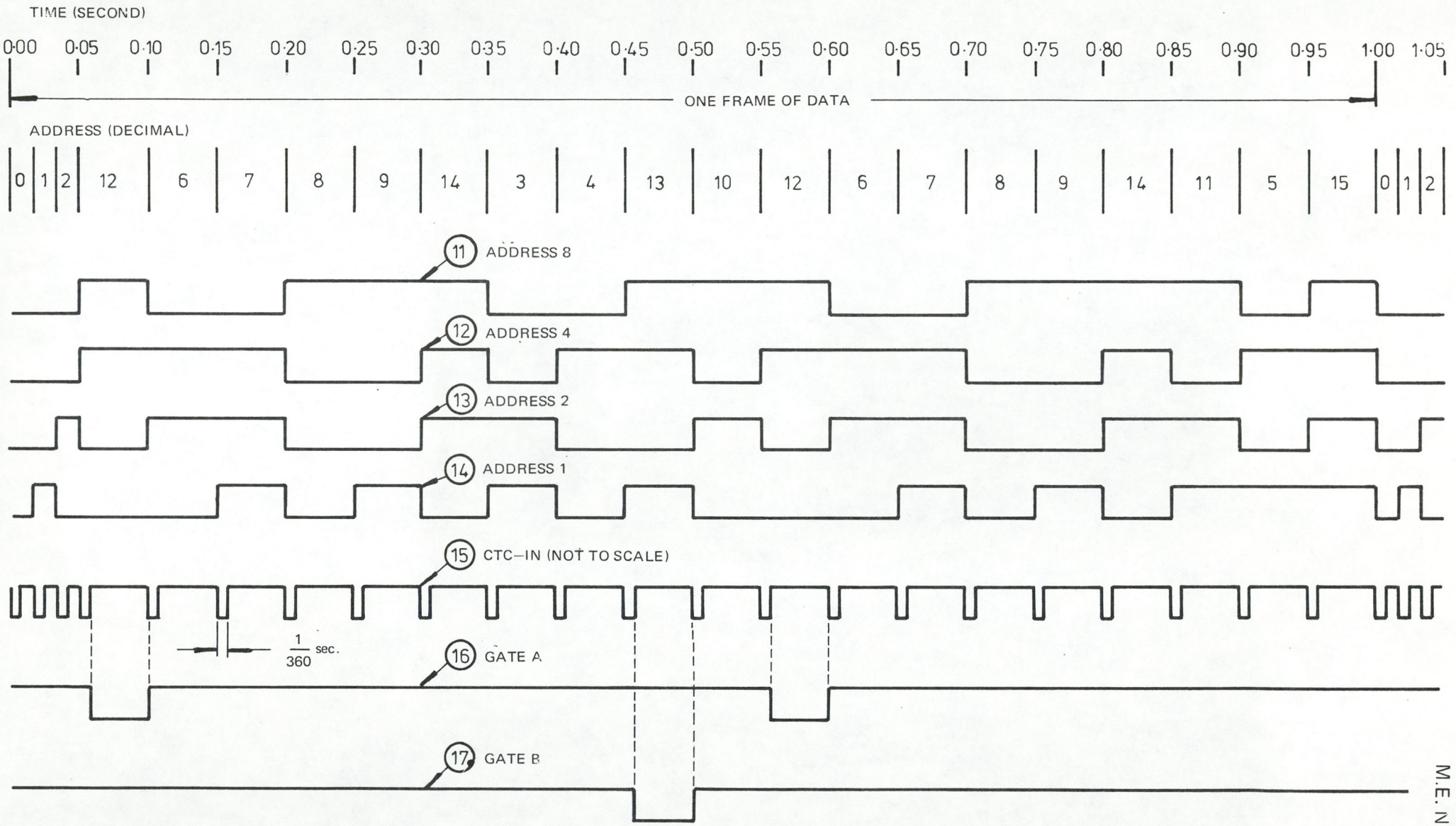


* REFER TO FIG. 2 FOR CIRCUIT LOCATION

FUEL FLOW INPUT CONDITIONER WAVEFORMS

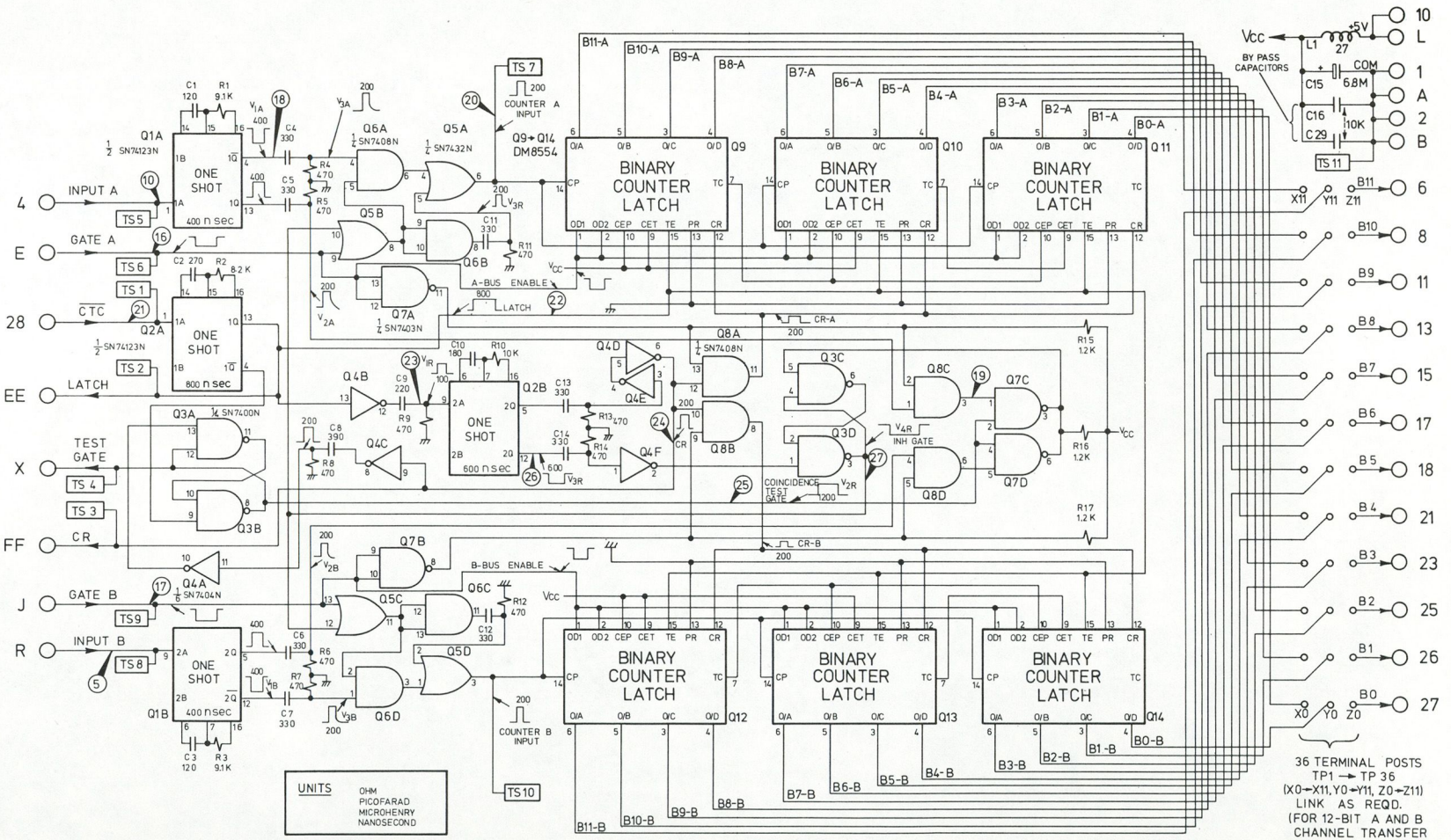


ENGINE SPEED INPUT CONDITIONER WAVEFORMS



INPUT ADDRESS DECODER WAVEFORMS

M.E. NOTE 354
FIG. 6



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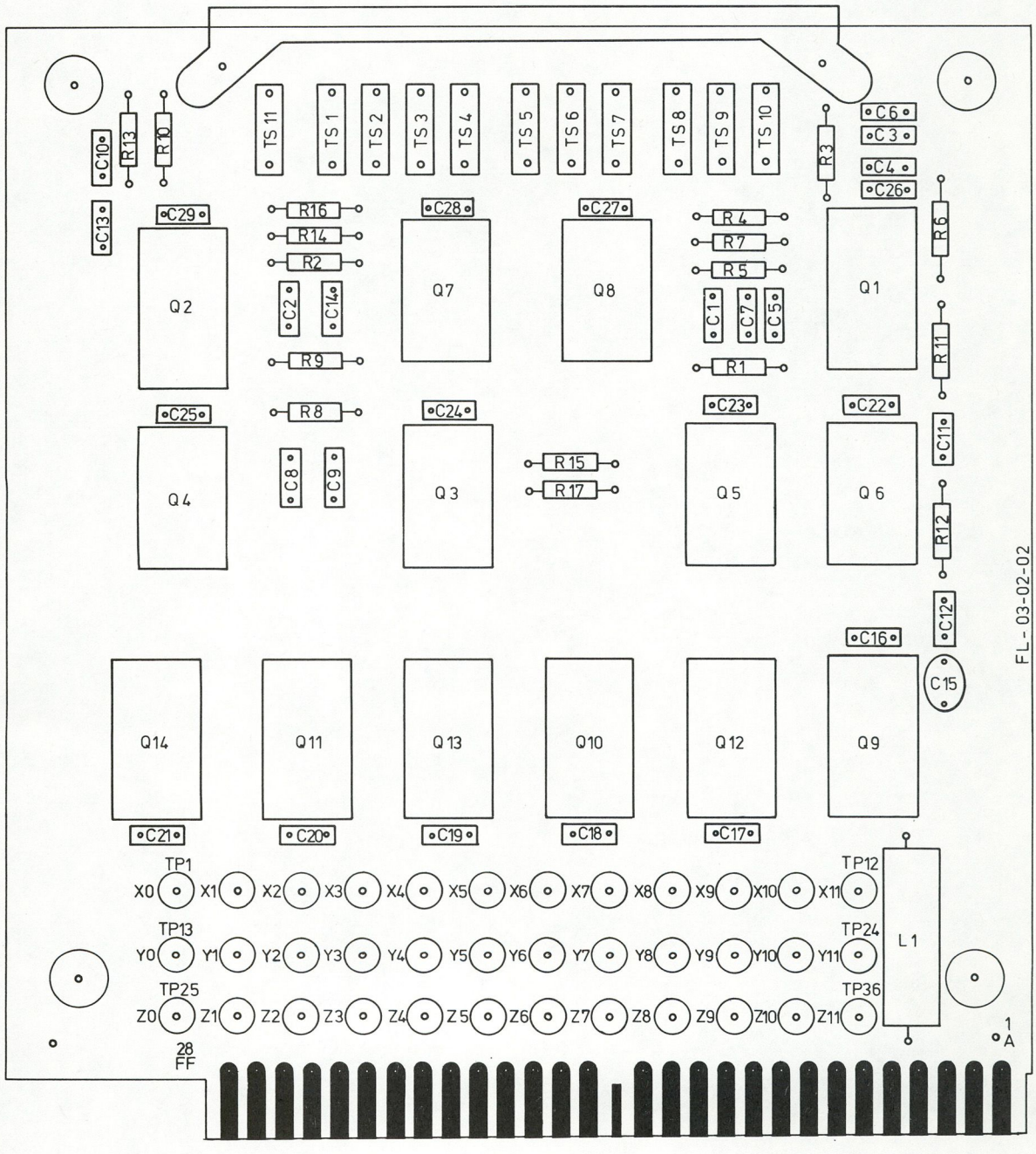
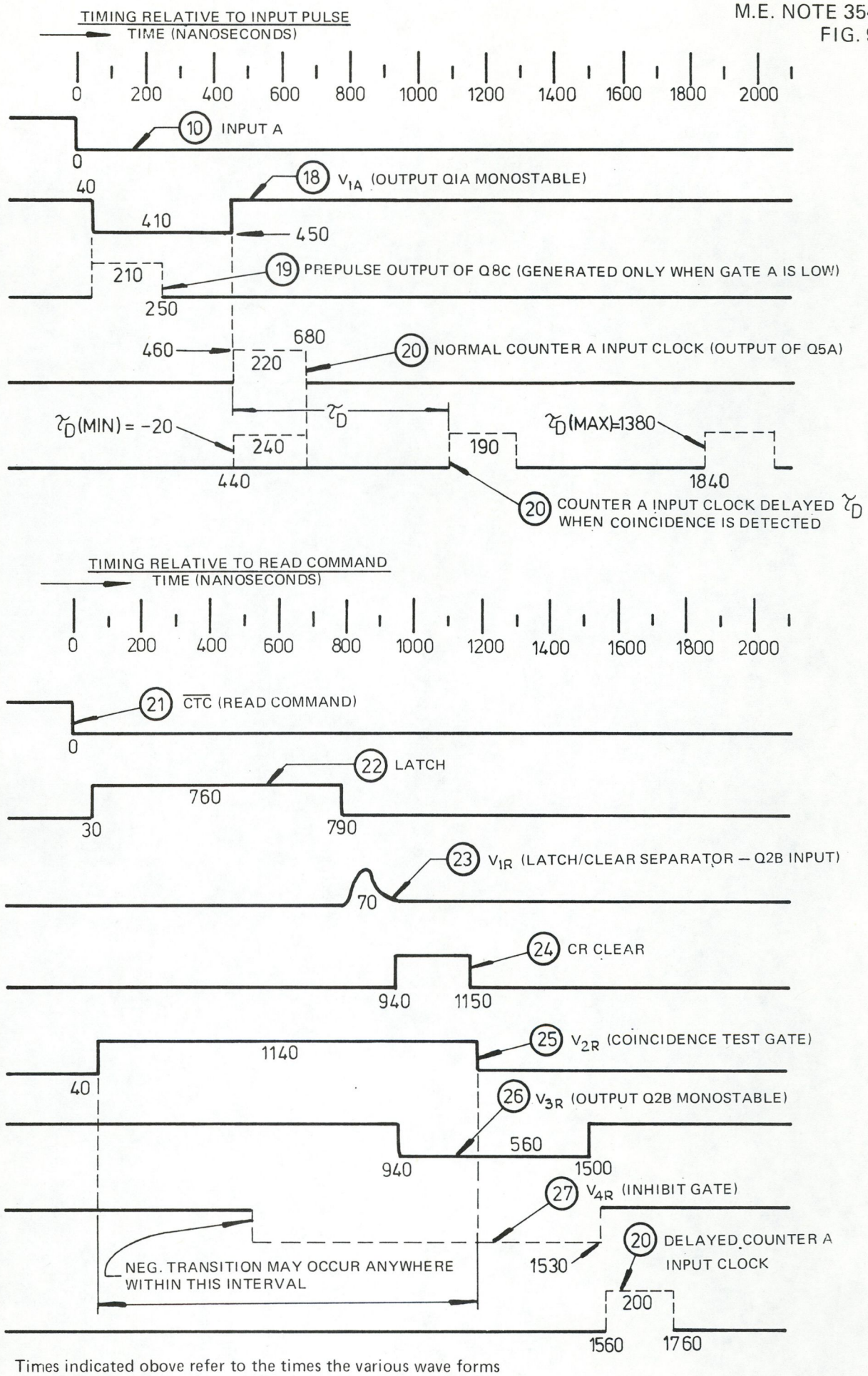
FREQUENCY TO DIGITAL CONVERTER

M.E. NOTE 354
FIG. 7

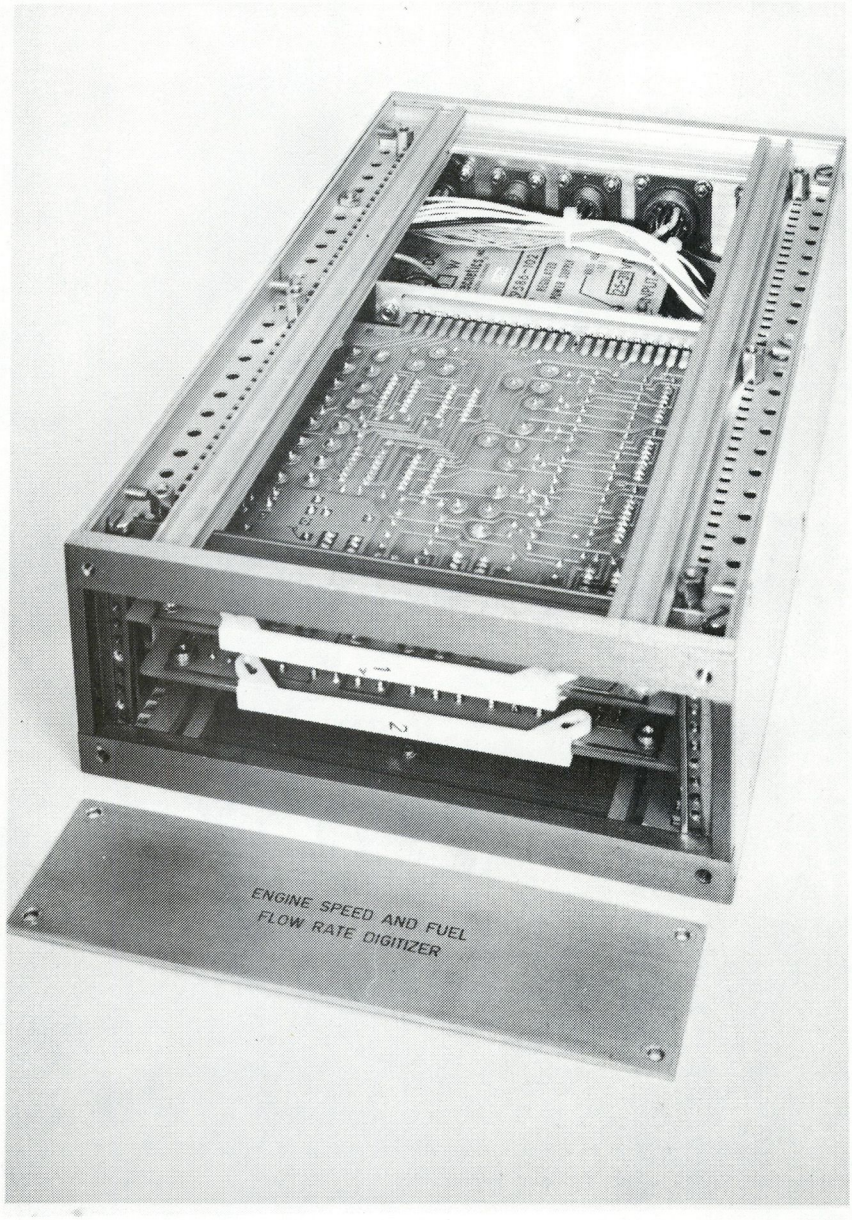


COMPONENT LAYOUT FOR FREQUENCY TO DIGITAL CONVERTER

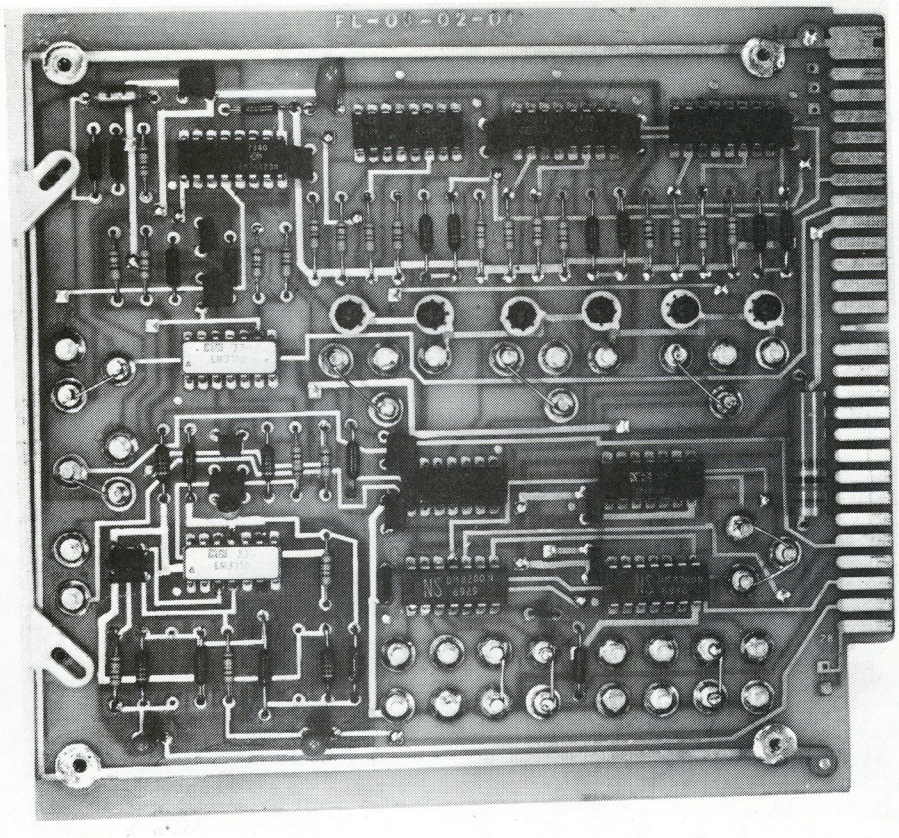


Times indicated above refer to the times the various wave forms pass the +1.5V level and are expressed in nanosecond. Any delays less than 50 nanosecond are due to device propagation delays.

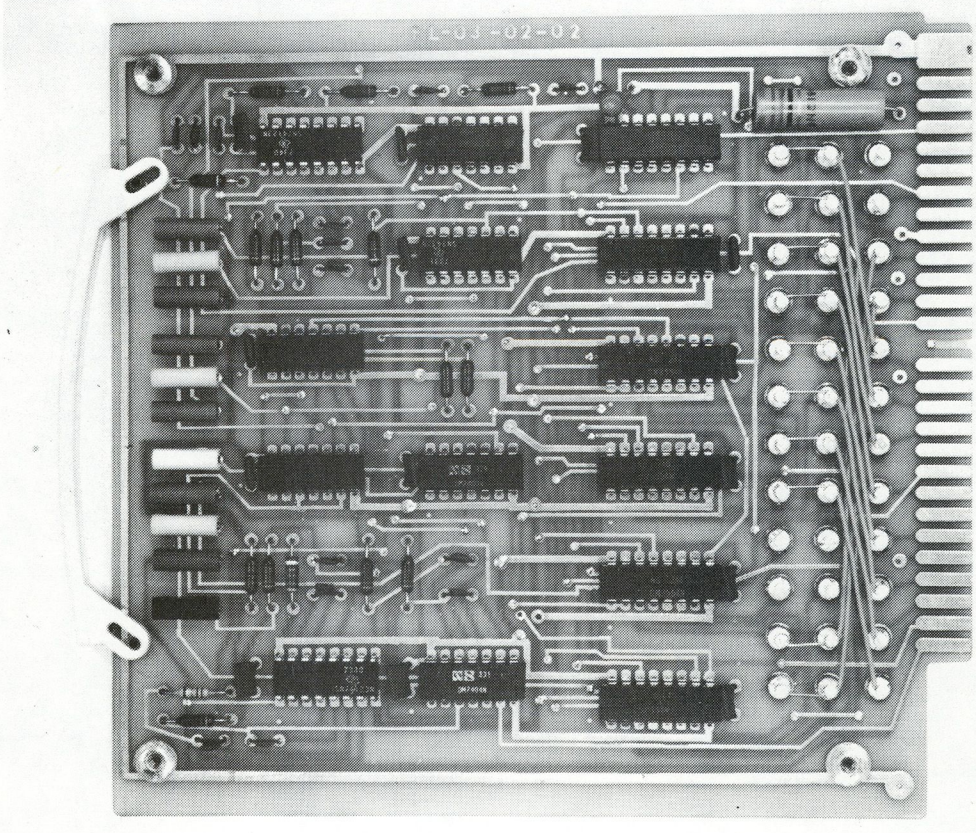
FREQUENCY TO DIGITAL CONVERTER WAVEFORMS



PHOTOGRAPH OF COMPLETED UNIT



(a) PHOTOGRAPH OF INPUT SIGNAL CONDITIONER CIRCUIT BOARD



(b) PHOTOGRAPH OF FREQUENCY TO DIGITAL CONVERTER CIRCUIT BOARD

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4. Title and Sub-Title AIRCRAFT ENGINE SPEED AND FUEL FLOW SIGNAL CONDITIONER WITH DIGITAL OUTPUT

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7. *ABSTRACT*

Engine speed and fuel flow rate sensors typically provide outputs in the form of a pulse train with repetition rate proportional to the measurand. Digitization of such data is readily accomplished by counting the number of pulses received per unit time. A conditioner which produces such digitization is described. It has the special property that no pulses are ever missed when the contents of the counter are transferred to associated data recording equipment. Thus the conditioner can be used for accurate totalizing of engine revolutions or fuel consumed over long periods.

8. Computer Program(s)—Titles and Language
Not applicable

9. Descriptors Digital techniques Flight instruments Aircraft instruments Fuel gauges Tachometers	11. Cosati Classifications 0104, 0902 12. Task Reference (RD/P) RD70/Air 72/11
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