REPORT
ARL/ME. 126

COMMONWEALTH OF AUSTRALIA

DEPARTMENT OF SUPPLY

AUSTRALIAN DEFENCE SCIENTIFIC SERVICE

AERONAUTICAL RESEARCH LABORATORIES

Mechanical Engineering Report 126

A DATA ACQUISITION SYSTEM SUITABLE FOR AIRBORNE APPLICATIONS

by

K. F. FRASER

July 1969

MELBOURNE

PRINTED BY DEPARTMENT OF SUPPLY, CENTRAL DRAWING OFFICE, MARIBYRNONG

DEPARTMENT OF SUPPLY

AUSTRALIAN DEFENCE SCIENTIFIC SERVICE

AERONAUTICAL RESEARCH LABORATORIES

MECHANICAL ENGINEERING REPORT 126

A DATA ACQUISITON SYSTEM SUITABLE FOR AIRBORNE APPLICATIONS

by

K. F. FRASER

SUMMARY

Techniques applicable to airborne data acquisition and recording are reviewed. From this review a system which allows simultaneous recording of analogue and digital data with a single analogue tape machine has been designed conceptually. Such a system offers many advantages over the other systems available for airborne data recording in Australia.

The system will accommodate with appropriate accuracy most data acquisition and recording requirements which arise in the testing of aircraft by the Aeronautical Research Laboratories. Simultaneous recording of flight crew commentaries on the same magnetic tape recorder is readily performed. Analysis of the recorded data requires the use of analogue replay equipment in conjunction with a digital computer.

CONTENTS

INTRODUCTION

In-flight data acquisition is an essential requirement for aircraft performance studies. With the many recent advances in magnetic tape handling equipment and computers it has become advantageous to store the acquired data on magnetic tapes. Detailed analysis of the data is usually performed later at a suitable ground station.

The magnetic tape recording instrument may be installed in the aircraft or may be situated at a ground station. In the latter instance radio telemetering of the data from the aircraft to the ground station is required. Generally the radio telemetering system is only applicable when the aircraft under study is in the vicinity of the ground station. The cost of the telemetering system tends to be prohibitive except for large scale research. If the magnetic tape recorder is installed in the aircraft it must be specially engineered to operate in the aircraft environment. A range of airborne magnetic tape recorders is now commercially available.

Aircraft evaluation studies involve the measurement of many physical quantities. Some quantities such as vibration displacement, noise and pressures at various points in jet engines are not normally required to be measured with extreme accuracy but frequently involve measurement over large bandwidths. Such data is usually recorded using analogue techniques. Other quantities such as airspeed, altitude, air temperature and engine speed frequently have to be measured with very high precision but usually over a relatively small bandwidth. High precision is required to enable basic computed quantities such as Mach Number and True Air Speed to be accurately evaluated and to enable small changes in performance to be indicated. Digital techniques must be employed for the recording of such data to the desired accuracy. Fortunately, in aircraft studies, large bandwidth and high precision are very rarely required simultaneously in a given measurement.

Magnetic tape recorders have been developed to a high degree of sophistication in both the analogue and the digital fields. However, the recorders have tended to be developed along different lines as the requirements are somewhat conflicting. Hence magnetic recorders are usually referred to as "analogue" or "digital." Generally analogue recorders require large recording bandwidths, good linearity, wide dynamic range and low crosstalk between channels. Staggered heads are invariably used to enable crosstalk between channels to be reduced sufficiently. Digital recorders, on the other hand, are usually designed to accept parallel data which, for high data packing densities, places very stringent requirements on azimuth alignment of the data on the tape. Invariably, digital recorders employ a single in-line headstack.

The trend to use separate machines for analogue and digital recording has been largely followed in aircraft studies. Larger aircraft can readily accommodate separate machines to record analogue and digital data. However, space limitations on many smaller aircraft, particularly military types, frequently do not allow the installation of separate recorders. In view of this latter application the concept of a "hybrid" recorder has evolved. The "hybrid" recorder is an analogue type recorder capable of simultaneously recording analogue and digital data.

This paper has been divided into two sections.

Section A is a review of the techniques applicable to airborne data acquisition and recording. From this review the need for simultaneous analogue and digital recording is established.

Section B relates to the hybrid recording system. Possible extensions of the analogue system of recording are indicated and a complete proposal for a digital recording system is given. The problems introduced when digital recording is performed on an analogue machine are described and analysed. Programme control requirements are developed and the logical sequences are derived for the digital system.

A scheme for seven channel parallel digital recording of data using the same analogue tape machine as used for the hybrid recording is also presented in Part B. For special applications in which only digital data is required such a system may be very useful.

PART A REVIEW OF TECHNIQUES APPLICABLE TO AIRBORNE DATA ACQUISITION AND RECORDING

A1. TECHNIQUES FOR RECORDING DATA ON MAGNETIC TAPE

There are five main systems of recording data on tape which will be considered, namely:

(1) Direct
(2) Carrier Erase
(3) Frequency Modulation
(4) Pulse Duration Modulation
(5) Pulse Code Modulation

The first four of these systems may be generally classified as "analogue" and the fifth system as "digital." The choice of a suitable recording system for each particular application will depend on the nature of the data to be recorded and the required accuracy. The characteristics of these systems of recording are detailed below.

A1.1. Direct

In this system the signal to be recorded is suitably amplified and mixed with a high frequency bias signal (Eldridge[1] and Bauer[2]). The combined signal is presented directly to the record head as a varying electrical current. The remanent flux density left on the tape is proportional to the magnitude of the signal current at the moment the tape passes the trailing edge of the record gap. Since the output from conventional reproduce heads is proportional to the rate of change of flux, DC data cannot be reproduced in the direct recording system. The practical lower frequency limit is approximately 50 hertz. The direct recording process has the advantage of providing the widest possible frequency range for any tape speed (Weber[3]). The limitations on the frequency response in direct recording are discussed by Danial, Axon and Frost,[4], Martin[5] and Borwick.[6]

The chief disadvantages of the direct recording system are:

(i) Recording of frequencies below about 50 hertz is not feasible.

(ii) Tape drop-outs which show up as loss of data or amplitude fluctuations seriously degrade the fidelity of the data recording. The effect is more serious at the higher recording frequencies. Franck[7] and Noble[8] discuss tape drop-outs in detail.

(iii) The dynamic range is relatively small (25 db for the Ampex Model AR 200 Airborne Analogue Tape Recorder available at these laboratories), particularly for the small track widths used in multi-channel data recording. Camras[9] shows that the noise varies as the square root of the track width whereas the signal level changes directly as the track width. Hence reducing a track width to half size reduces the signal to noise ratio by 3 db. Noise is inherent in the magnetic recording process and cannot be eliminated. For further details on tape noise refer to Howling,[10] Snow[11] and Moris.[12]

(iv) Crosstalk between adjacent channels becomes quite high as the recorded wavelengths are increased (16 db at 110 hertz and 60 inches per second [ips] for the Ampex Model AR 200 Tape Recorder).

(v) The overall accuracy attainable is fairly low. An accuracy of 5% can be achieved but 10% is probably a more realistic figure.

(vi) Godinez and Muench,[13] and Wainwright,[14] show that the direct recording technique produces considerable phase distortion unless special corrections are made. The problem of phase distortion arises because of the nature of the head plus tape characteristic. The replay head senses the rate of change of flux and hence the amplitude characteristic has a 6 db per octave upward slope. When the wavelength on the tape approaches the width of the reproduce head gap the replay amplitude starts to decrease. However, this drop in amplitude is not accompanied by a phase shift. When compensation (using linear networks) is used on replay to compensate for this "gap effect" phase shifts are introduced which produce phase distortion. Various systems of phase correction as indicated by Godinez and Muench,[13] and Wainwright,[14] can be employed.

Most instrumentation recorders (as distinct from audio recorders) provide a record characteristic (record head current versus frequency) which is flat over the specified frequency band. In contrast most audio recorders pre-emphasize the high frequencies, and sometimes the low frequencies, prior to recording. Such pre-emphasis is quite permissible in audio recorders where it can be assumed that components at the extremes of the audio band will always be of relatively low level. Because of the pre-emphasis audio recorders frequently have better specifications with respect to frequency response and signal to noise ratio than instrumentation recorders operated at the same speed.

A1.2. Carrier Erase

The carrier erase system of recording, discussed by Work and Lewis,[15] is a slight modification of the direct recording system. Prior to the acquisition of data a carrier is recorded on the tape and during acquisition the data signal erases a portion of the pre-recorded carrier. An amplitude modulated signal appears on the replay head. Usually the carrier is recorded at sufficient amplitude to saturate the tape. The erase curve is not completely linear but it is possible to choose a fairly linear portion for the operating range. DC bias is applied during the recording of the data so as to place the operating point centrally on the linear portion of the erase curve. To re-establish the data signal on replay an amplitude demodulator is required.

The carrier erase system is subject to the limitations associated with the direct recording system except that bandwidth is traded for the ability to record down to DC. The maximum data frequency is limited to approximately one-sixth of the carrier frequency. Bandwidths obtainable are comparable with those achieved using wideband frequency modulation (FM) recording techniques. Amplitudes in the carrier erase system are not affected by noise and tape speed variations to the same extent as in the FM system. In other respects the performance is inferior to wideband FM recording, accuracies no better than 5 to 10% being obtainable.

A1.3. Frequency Modulation

There are two main systems of frequency modulation (FM) recording in common usage, the wideband system and the narrow band system (IRIG[16] and Godinez[17]). In the wideband FM recording system the chosen carrier is deviated by the modulating signal up to $\pm 40\%$ of the carrier frequency whereas in the narrow band system the carrier is deviated up to $\pm 7{\cdot}5\%$ of the carrier frequency ($\pm 15\%$ is also sometimes used). The FM recording technique overcomes the two basic limitations of the direct recording process namely the inability to record down to DC and the amplitude instability caused by tape drop-outs. The problem of phase distortion which arises in the direct recording system is absent in the FM recording system as the non-linear phase characteristic of the tape recorder is not significant (Godinez and Muench[15]).

Tape speed variations are generally referred to as "wow" and "flutter" where "wow" refers to variations of a few hertz or less and "flutter" refers to variations at a higher frequency. The variations show up as noise on the replay channel (Godinez,[18] Disbray[19] and Pear[20]) and hence it is imperative that they be kept to a minimum for FM recording. In the wideband system a 1% deviation in frequency resulting from flutter and wow in the tape transport would appear as a $100/40 = 2{\cdot}5\%$ noise signal, whereas in the narrow band system the corresponding noise signal would be $100/7{\cdot}5 = 13{\cdot}3\%$

Normally the carrier frequency is placed at approximately the peak of the head to tape response curve (Fig. 1). Under these conditions, if the noise resulting from flutter and wow is neglected, the carrier can be reproduced fairly easily with a 40 db signal to noise ratio. Godinez[21, 22] shows that an analytical relationship exists between the signal to noise ratio of the FM carrier and the signal to noise ratio of the demodulated FM data.

$$\left(\frac{S}{N}\right)_{\substack{\text{DEMOD.}\\ \text{FM}}} = 3\beta^2 \left(\frac{S}{N}\right)_{\text{CARRIER}}$$

where $\beta = \dfrac{\text{deviation frequency}}{\text{data bandwidth}} \left(\begin{matrix}\text{modulation}\\ \text{index}\end{matrix}\right)$

For extended bandwidth operation $\beta \simeq 2$.

$$\left(\frac{S}{N}\right)_{\substack{\text{DEMOD.}\\ \text{FM}}} = 12\left(\frac{S}{N}\right)_{\text{CARRIER}}$$

That is a 12 times improvement in signal to noise ratio (once again neglecting the effects of flutter and wow).

At β's less than 0·57 the signal to noise ratio of the FM data will be lower than the signal to noise ratio of the carrier.

Godinez[22] shows that greatly extended bandwidth FM may be achieved at the expense of reduced signal to noise ratio if micro-gap reproduce heads (30 micro inch say) are used and if the carrier is placed beyond the peak of the head to tape response (say at the 20 db down point). The table below shows a comparison between the standard IRIG system and the extended bandwidth system referred to above.

Tape Speed	IRIG FM			Extended Bandwidth FM		
	Carrier	Bandwidth	Signal to Noise Ratio	Carrier	Bandwidth	Signal to Noise Ratio
30 ips	27 KHz	0–5 KHz	42 db	225 KHz	0–100 KHz	30 db
60 ips	54 KHz	0–10 KHz	42 db	450 KHz	0–200 KHz	30 db

In the wideband system modulation frequencies up to 20% of the carrier frequency may be accommodated (IRIG[16], page 37). For the greatly extended bandwidth FM system referred to in the previous paragraph a higher modulation index is used.

In the wideband system (deviation $\pm 40\%$ of the carrier frequency) of FM recording, the system most widely used, accuracies of about 2% can be readily achieved.

The following is a summary of the advantages as applied to the wideband system of FM recording:

(i) Recording of data down to DC is possible.

(ii) Amplitude instability caused by tape drop-outs does not significantly degrade the overall accuracy.

(iii) Data signals can be readily reproduced with high signal to noise ratios (greater than 40 db).

(iv) Moderately large data bandwidths can be accommodated. It is relatively easy to obtain a flat frequency response over the specified bandwidth.

(v) The non-linear phase characteristic of the tape recorder does not give rise to phase distortion.

(vi) Data can be readily recorded and reproduced with good accuracy (2%).

(vii) Crosstalk between adjacent channels is relatively low.

The chief disadvantage of FM recording is that tape speed variations between record and replay show up as noise on the demodulated data. Hence high demands are placed on the tape speed stability of record and replay machines.

A1.4. Pulse Duration Modulation

In the pulse duration modulation (PDM) system of recording the data is sampled at discrete intervals and the duration of a pulse is made proportional to the level of the data signal at the

time of sampling. For discussion on the PDM record system refer to Weber,[3] IRIG,[16] Axon,[23] Borwick[24] and Halfhill.[25] Normally a number of data channels are multiplexed on a time division basis in this system of recording. Time division multiplexing of three data signals is illustrated in Fig. 2. The unit which converts a voltage level to a proportional pulse duration is called a "keyer." The PDM waveform appearing at the output of the keyer is differentiated by the record amplifier so that only the leading and the trailing edges of the pulses are recorded on the tape. On replay a normal PDM waveform is reconstructed by means of the reproduce amplifier. The PDM waveform is converted to a pulse height waveform by a de-keying unit. Individual channels are separated by means of a de-multiplexer. For any given channel the output from the de-multiplexer is discontinuous. By passing the output through a suitable filter a smooth waveform virtually identical to the recorded data waveform results.

The standard keying rate of 900 per second has been set by the Inter-Range Instrumentation Group[16] for telemetry and tape recording. Any combination of number of sampled parameters and channel sampling rate may be employed provided 900 per second keying rate is maintained (e.g. 90 × 10, 45 × 20, 30 × 30, etc.). Normally one or two channels of the multiplexer are used for frame synchronization and two for zero and full scale calibration signals. Frame synchronization pulses must be recorded to enable the ground station data reduction equipment to identify channels.

At least six samples per cycle of a sinewave are required in order to enable accurate reconstruction to be made. The upper frequency limit of the data to be recorded will therefore be approximately one-sixth of the sampling rate for a particular channel. For channels which are sampled once per scan of the multiplexer the following table applies:

Multiplexer		Signal Information	
Number of Channels	Speed in Complete Scans per Second	Number of Channels*	Upper Frequency Limit-Hertz
90	10	86	1·7
45	20	41	3·3
30	30	26	5
20	45	16	7·5
10	90	6	15
1	900	1†	150

* Allowing two multiplexer channels for synchronization purposes and two for calibration (except †).

† No synchronizing pulses required, also no calibration signals have been included.

To obtain a better frequency response for a particular information channel it is possible to utilize more than one multiplexer channel and hence achieve a higher effective sampling rate for that information channel.

The pulse durations normally used are tabulated below:

Input Signal Voltage	Pulse Duration
0	90 microsecond
5 volts (Full Scale)	660 microsecond

The total interval available between samples is 1100 microsecond approximately and the dynamic range according to the above table is 570 microsecond.

The precision with which the pulse duration may be recorded will be dependent on the tape speed employed and hence the overall accuracy will be degraded at the lower tape speeds assuming that the standard 900 per second sampling rate is invariant. Weber[3] states that the PDM process is capable of recording an effective 40 sinewave cycles per inch of tape. Assuming that six samples are required per cycle then the 40 sinewave cycles per inch of tape would be equivalent to 240 samples per inch. The latter figure corresponds to the normal keying rate (900 per second) at a tape speed of $3\frac{3}{4}$ inches per second ($900/3\frac{3}{4} = 240$). Systems conforming to IRIG specifications (IRIG[16] Sec. 6.4.5) are required to have the characteristics tabulated below:

Tape Speed inch per second	Minimum Pulse Duration microsecond	Accuracy microsecond
60	75	±2
30	75	±2
15	100	±3

Assuming a dynamic range of 570 microsecond an accuracy of approximately ±2/570 (0·35%) should be attainable at 30 ips and 60 ips and an accuracy of ±3/370 (0·53%) should be attainable at 15 ips. Generally an accuracy of better than 1% is attributed to the PDM system but as outlined above this will be dependent on tape speed. Referring to the above table it is to be noted that the minimum pulse duration which may be used increases as tape speed is reduced. Even at 15 ips the IRIG specification gives a figure of 100 microsecond for minimum pulse duration which is slightly greater than the 90 microsecond typically used as the zero input equivalent pulse duration. The limitation of minimum pulse duration arises because sufficient time has to be allowed for the leading edge replay pulse to decay (Fig. 3) before the trailing edge pulse appears. Hence minimum pulse duration will represent a major limitation at the lower tape speeds.

Tape flutter and wow present less problems in the PDM system than in the FM system. Only the integrated flutter and wow timing error over the pulse duration time is of significance.

Generally the PDM system is very useful for recording, at better than 1% accuracy, a multiplicity of data signals having relatively low frequency content.

A1.5. Pulse Code Modulation

In the pulse code modulation (abbreviated as PCM and also referred to as "digital") system of recording, the data is converted to a code consisting of a series or group of binary digits which are recorded on tape (Weber,[3] Halfhill,[25] Godinez,[26] and Leach Corp.[27]). The heart of the pulse code modulator is the analogue to digital converter (frequently abbreviated as ADC) which converts the analogue outputs from the transducers into a digital form. Normally a sampling technique, similar to that for PDM, is used to enable time multiplexing of a number of channels. For the high sampling rates normally used a solid state multiplexer is the obvious choice. Accuracy in the digital system, with the exception of occasional erroneous output data due to tape dropouts, is not dependent on the tape record/replay system (unlike all the forms of analogue recording) but depends only on the characteristics of the ADC and the multiplexer. The possible accuracy of the digital recording system depends on the resolution of the ADC as indicated in the following table:

Number of Binary Digits	Possible Accuracy
5	1 part in 2^5 (or 32) 3%
7	1 part in 2^7 (or 128) 1%
10	1 part in 2^{10} (or 1024) 0·1%

Data may be recorded in serial form on one or more tracks or may be recorded in parallel on multiple tracks. Digital recording is accomplished by magnetizing the tape to saturation in both directions in one of the following ways (Weber[3] and Godinez[26]):

(i) **Return to Bias** (RB)

The tape is magnetically biased to a predetermined level in one direction (say $-$) and the "ones" are recorded by magnetizing the tape in the opposite polarity (Fig. 4(a)). After each pulse for a "one" the tape returns to the bias condition.

(ii) **Return to Zero** (RZ)

The tape is normally in a demagnetized state and "ones" and "zeros" are assigned opposite polarities. A pulse is recorded for each digit (Fig. 4(b)).

(iii) **Non Return to Zero—Change** NRZ(C)

The tape is always saturated in one direction or the other, the reversals in polarity occurring each time a change in bits occurs (Fig. 4(c)).

(iv) **Non Return to Zero—Mark** NRZ(M)

Polarity is reversed each time a "one" is recorded (Fig. 4(d)).

(v) **Manchester Code** (also referred to as Ferranti Code or Phase Modulation)

The clock is mixed with the data before recording (Fig. 4(e)). By eliminating the long intervals when no transition occurs (as may occur in NRZ) a higher degree of immunity against tape dropouts results.

Godinez[26] compares the various recording techniques for rugged environment conditions. He provides the following comparison table.

Recording Technique	Maximum Packing Density	Dropout Accuracy	Comments
RB	600 bit/inch	1×10^5	(1) Inefficient bandwidth utilization (2) Poorest of record systems
RZ	300 bit/inch	1×10^6	(1) Lowest bandwidth utilization
NRZ(C)	600 bit/inch 1000 bit/inch 2000 bit/inch	1×10^6 1×10^5 1×10^4	(1) IRIG standard for recording (2) Simple electronics (3) Accuracy dependent on packing density
NRZ(M)	600 bit/inch 1000 bit/inch 2000 bit/inch	$0{\cdot}5 \times 10^6$ $0{\cdot}5 \times 10^5$ $0{\cdot}5 \times 10^4$	(1) Often used recording method (2) Slightly better than NRZ(C) in accuracy
Manchester Code	1000 bit/inch 800 bit/inch	1×10^7 1×10^8	(1) Most accurate recording scheme (2) More complex electronics (3) Density limited to under 1000 bit/inch

The PCM system places stringent demands on tape uniformity and head to tape contact (Weber[3]) to minimize tape dropouts (Franck[7]). The latter condition requires an extremely fine finish on the surface of the head, adequate tape pressure and a minimum tendency of the head to collect oxide particles from the surface of the tape. Some degree of immunity from tape dropouts is achieved by means of redundant check (or parity) characters. Another aspect which requires careful attention if characters are recorded in parallel is that of tape skew which arises if the centre line of the tape departs from a perpendicular to the line of record and reproduce head gaps. The problem becomes a major one at high packing densities as corresponding bits on different tracks tend to become misaligned.

The PCM system of recording is relatively insensitive to wow and flutter in the tape transport. It provides the greatest accuracy of all the recording systems. To achieve the high overall accuracy the transducers, multiplexer and ADC must each have high precision.

A1.6. Comparison of Recording Techniques

A comparison of the various recording systems is made in the following table (overleaf).

COMPARISONS OF RECORDING PROCESSES

Characteristic	Direct	Carrier Erase	FM (Standard Wideband)	PDM	PCM
Low frequency limit	50 Hz at $7\frac{1}{2}$ ips 300 Hz at 60 ips	0 Hz	0 Hz	0 Hz	0 Hz
High frequency limit	250 KHz at 60 ips 125 KHz at 30 ips 60 KHz at 15 ips	10 KHz at 60 ips 5 KHz at 30 ips 2·5 KHz at 15 ips	20 KHz at 60 ips 10 KHz at 30 ips 5 KHz at 15 ips	Approx. $150/n$ at $3\frac{3}{4}$ ips where n is number of channels	Up to approx. $80/n$ Hz at 30 ips for system proposed (n = No. of channels)
Figure of merit (cycles per inch)	4160	166	333	40	3
Effect of 1% change in tape speed	1% change in frequency. Small change in amplitude	1% change in frequency. Small change in amplitude	2·5% error signal	1% magnitude error	None
Dynamic range	25 db typical	20 db typical	46 db typical	52 db typical	No noise introduced in the recording process
Channels per track	Usually one, several with frequency multiplexing	Usually one	Usually One	Up to 86 channels time multiplexed	Any number may be time multiplexed
Accuracy	5–10%	5–10%	2%	1%	0·1% Typical
Linearity	5%	5%	1%	0·5% Typical	Depends on ADC. Best linearity of all systems
Effect of tape dropouts	Produces large amplitude changes	Produces large amplitude changes	Very little effect	Normally no effect	May give erroneous readings. This system requires minimum dropouts
Crosstalk between adjacent channels	Quite high at low frequencies and high tape speeds	Low	Very low	Nil	Nil
Circuit complexity	Simple	Simple	Moderate	Complex	Complex

A2. TECHNIQUES SUITABLE FOR USE IN AIRBORNE DATA RECOORDING

Some of the measurements likely to be required in aircraft performance studies are summarized below and the appropriate recording techniques are indicated.

(i) Frequency Range 50 Hz to 250 KHz, Accuracy 10%

Voice which is normally recorded in conjunction with data falls in this category as very low frequency response is not required and 10% accuracy is quite adequate.

Occasional input signals with very high upper frequency limit (up to 50 KHz) arising in the measurement of vibrations and noise on jet engines need to be recorded.

Direct recording techniques are normally used for voice recording and must be used for the high frequency vibration recording.

(ii) Frequency Range 0 to 20 KHz, Accuracy 2%

Most vibration measurements fall into this category. Vibration frequencies as low as 2 Hz are quite common. Usually an accuracy of 2% is adequate for vibration measurement, whereas the 10% accuracy offered by the direct recording system is generally unacceptable.

Pressure measurements ranging from static to dynamic with high frequency content also fall in this category.

Noise measurements requiring better accuracy and better low frequency performance than that obtainable using direct recording techniques also fall into this category.

Other quantities requiring measurement down to DC are temperature, force, strain and the like.

Wideband FM techniques (1 channel per track) are normally used for the recording of these quantities.

(iii) Frequency Range 0 to 150 Hz (based on 1 information channel, proportionately lower for a greater number of channels), Accuracy 1%.

There are a large number of measurements to be made on aircraft which involve signals that can be regarded as static or quasi-static. Some of these are:

(a) Pressures
(b) Temperatures
(c) Control surface angles
(d) Strains, forces and loads (picked up from strain gages)
(e) Aircraft pitch, roll and yaw (picked up from gyros)
(f) Aircraft heading (picked up from compass)

A large number of these quantities may require measurement during any given test and time division multiplexing is desired. PDM techniques can be readily used for these measurements.

It is to be noted that the standard keying rate of 900 per second for the PDM system as specified by IRIG[16] limits the upper frequency limit to approximately 150 Hz for one information channel. However, this response is feasible at $3\frac{3}{4}$ ips tape speed. Higher keying rates at higher tape speeds would allow increased data signal bandwidths to be obtained.

Many measurements which can be recorded using PDM techniques can also be recorded more accurately using PCM techniques. However, the PDM system offers higher information packing density on the tape than the PCM system (40 cycle per inch as compared with 3 cycle per inch). If the IRIG standard keying rate is used then the frequency response obtainable at $3\frac{3}{4}$ ips for the PDM system would be approximately the same as that obtainable at 60 ips for the PCM system referred to below.

(iv) Frequency Range 0 to 150 Hz (based on one information channel, proportionately lower than for a greater number of channels), Accuracy 0·1%.

A small number of flight parameters including airspeed, altitude, air temperature, jet pipe temperature, engine speed and fuel flow often require measurement to high accuracy. High precision is required because basic computed quantities such as true airspeed, Mach number, rate of climb, overall drag and net thrust are functions of several of these parameters, and if the final answers are to be sufficiently accurate, and especially if one is looking for small improvements or changes in performance, then no lower precision is acceptable. PCM (digital) recording is the only feasible method of achieving the required accuracy.

The bandwidth of approximately 150 Hz is that obtainable for one channel of serial digital data recorded at 60 ips tape speed. Proportionately lower bandwidths would be obtained at lower tape speeds.

A3. SIGNAL CONDITIONING REQUIREMENTS RELEVANT TO AIRBORNE DATA RECORDING

A3.1. Transducers and Associated Signal Conditioning Equipment

The function of the signal conditioning equipment is to accept the "raw" input data signals, usually derived from suitable transducers, and provide outputs acceptable to the tape recorder. Such functions as amplification, attenuation, zero shifting, impedance changing and filtering are required of the signal conditioning equipment. So that tape recorder plug-ins may be interchanged in the field without the need for re-alignment it is desirable that 100% input level to the tape recorders be rationalized to a standard level (1 volt R.M.S. seems to be a generally adopted standard). Hence it is the function of the signal conditioning equipment to provide outputs for the tape recorders based on the standard 100% level.

The tape recorder inputs are usually single ended (one side is connected to case which is in turn connected to the recorder supply common). Normally the outputs of the signal conditioning equipment are connected to the tape recorder input via co-axial cable. The co-axial cable connection provides good immunity from pick-up but in situations where the signal conditioning equipment is placed remotely from the tape recorder the shunt capacitance may be quite significant. So that satisfactory operation may be obtained in such cases it is essential that the output of the signal conditioning equipment be unaffected by moderate capacitance loading (50 feet of co-axial cable at 30 pF per foot giving a total of 1500 pF should be accommodated).

The minimum impedance as seen at the recorder inputs is typically 10 kilohm and hence the output impedance of the signal conditioning equipment should be low in comparison. Another reason why the output impedance of the signal conditioning equipment should be kept low is to prevent high frequency roll-off because of the capacitance loading. To meet these requirements the output impedance of the signal conditioning equipment should normally be kept below about 100 ohm.

A wide variety of transducers is required for use in the measurement of physical quantities such as pressure, temperature, displacement, velocity and acceleration. Invariably the transducers provide an electrical output. Normally the output is a direct analogue of the physical quantity being measured but transducers having digital output have also become available in recent years. Transducers may be broadly classified according to their principle of operation. Some of the more common types of transducer will now be briefly considered with a view to indicating the signal conditioning requirements.

(i) **Potentiometer Type**

In this type of transducer a change in the physical quantity being measured causes the wiper of a precision potentiometer to be displaced. A typical application is in the measurement of relatively large linear or angular displacements.

The potentiometer type transducer requires a stable DC or AC supply. Usually the full scale output of these devices is sufficient to allow direct connection to the tape recorder input.

(ii) **Strain Gage Type**

The strain gage transducer is used for the measurement of a large number of physical parameters such as displacement, acceleration, force, pressure and the like. The most commonly used strain gage transducer has an unbonded wire filament strain gage which forms the active arm of a Wheatstone Bridge circuit. The strain gage bridge is supplied with stable DC or AC, typically about 5 volt, and the bridge output is typically about 5 millivolt full scale.

The outputs from wire strain gage transducers require amplification before being taken to the tape recorder inputs. In Fig. 5(a) a typical strain gage bridge has been drawn. An amplifier having a single ended input may be used if a completely isolated supply is used for the bridge. However, such an arrangement does not permit more than one strain gage transducer to be operated from any given bridge supply. A better solution is to use an amplifier having a differential input. Under these conditions one side of the bridge supply may be connected to the amplifier common and hence a number of transducers may be operated from the one supply. In addition a differential input amplifier has much lower drift than an amplifier with single ended input if a chopper is not used. Drift is a very important consideration when the transducer is excited from DC and response down to DC is required. In Fig. 5(b) a method of connecting the bridge circuit to a high gain amplifier with differential input is illustrated.

If the bridge, which is considered to be initially balanced, is unbalanced by αR in one arm, then, referring to Fig. 5(a), the open circuit output voltage V_D is given by

$$V_D = \left(\frac{1+\alpha}{2+\alpha} - \tfrac{1}{2}\right) V_S$$

$$= \frac{\alpha}{4(1+\alpha/2)} V_S$$

$$\simeq \frac{\alpha}{4} V_S \qquad \text{for } \alpha \ll 1 \text{ which is usually a good approximation.}$$

If the bridge having this same unbalance is connected to the amplifier as indicated in Fig. 5(b) then the output voltage will be given approximately by

$$e_0 = 2nV_D$$

$$= \frac{\alpha n V_S}{2} \qquad \text{assuming } \alpha \ll 1 \text{ and } n \gg 1.$$

The amplifier must have high common mode rejection and for strain gages supplied with DC it is essential that the amplifier drift be very low.

Semiconductor strain gages having much higher outputs than the conventional wire gage are also available. The linearity of the semiconductor type is, however, not as good as the wire type.

(iii) **Capacitance Type**

In capacitance type transducers the capacitance of the sensing element varies with the measurand. In order to obtain an electrical output it is necessary to supply an external voltage to the transducer. One method for obtaining the requisite output is to use an AC bridge. Another method uses the transducer capacitance change to vary the frequency of an oscillator. Such quantities as displacement (proximity type transducer), pressure, temperature and the like may be measured with this type of transducer. Response down to DC is possible.

(iv) **Piezo Electric Type**

In this type of transducer which utilizes the piezo-electric effect the charge on a crystal (which appears electrically as a capacitor) varies with the measurand. The transducer is a self-generating type and therefore requires no external voltage supply. It is used frequently for the measurement of acceleration, pressure, sound level and the like. Since piezo-electric transducers generate charge proportional to the measurand, the voltage as seen at the transducer terminals will depend on the capacitance loading. Response down to DC is not possible, the lower cut-off frequency being determined by the value of the effective shunt capacitance and resistance components as seen at the transducer terminals. Frequently high input impedance voltage amplifiers are used in conjunction with these transducers to provide the necessary amplification and impedance change. In such instances transducer re calibration is necessary whenever the capacitance loading on the transducer is changed such as occurs if a different connecting cable is used.

Charge amplifiers (amplifiers which provide an output voltage proportional to input charge) provide the best form of signal conditioning equipment for use with piezo-electric transducers as transducer calibration is unaffected by changes in the shunt capacitance across the transducer. Very low cut-off frequencies of the order of a small fraction of 1 Hz are fairly easily achieved when charge amplifiers are used.

(v) **Inductance Type**

Three main types of inductive transducer, the velocity type, the variable reluctance type and the linear variable differential transformer (L.V.D.T.) type will be considered.

The velocity type transducer is self generating. Motion of a magnet within a coil generates an output voltage proportional to the velocity of the magnet relative to the coil. Such transducers are used for measuring velocity and are frequently used in vibration work. Sensitivities covering a broad range are available and are typically some hundreds of millivolts full scale for vibration transducers. Some amplification is usually required to bring the signals to a level suitable for most tape recorders. Typically an AC amplifier with a gain of up to 20 and an input impedance of approximately 10,000 ohm would satisfy most requirements.

In the variable reluctance type of transducer a slug of magnetic material moves between two coils. Changing the slug position changes the reluctance of the coils which in turn changes the impedance of an electrical circuit in which the coils are connected. Such transducers require

AC excitation. Frequently the variable reluctance type transducer is used for measuring displacement and pressure. These transducers are usually small, have fast response time and show good immunity from shock and vibration. Response down to DC is possible. The signal conditioning equipment required consists of an oscillator (of frequency at least 10 times that of the maximum frequency of interest of the measurand) and an amplifier having a phase sensitive demodulator. Usually the output is relatively high and little amplification is required.

In the L.V.D.T. type of transducer the sensing element moves an armature inside the three coils of a differential transformer. One of the coils (called the primary coil) is energized with AC. The coupling from the primary coil to each of the other two coils (called the secondary coils) is changed equally but in opposite senses due to a displacement of the armature. The L.V.D.T. requires AC excitation of a specific frequency which is usually relatively low (50 Hz, 60 Hz, and 400 Hz are typical). Any given L.V.D.T. requires to be matched to the associated signal conditioning equipment. Response down to DC is possible. A phase sensitive demodulator is required to give an output voltage which is the analogue of the measurand. The output of the L.V.D.T. is usually quite high, the shock and vibration immunity poor, and the frequency response low (less than 40 Hz). The L.V.D.T. type of transducer is used mainly for the measurement of displacement and pressure.

(vi) **Thermocouple Type**

The thermocouple type transducer employs the Seebeck effect (i.e. an e.m.f., produced in a circuit containing two conductors having two junctions at different temperatures, varies with temperature difference between the junctions). This type of transducer is frequently used for the measurement of temperature. Usually the thermocouple itself contains only one junction (often referred to as the "hot" junction). In order to measure temperature a "cold" junction which is held at a fixed temperature (usually 0 °C) or a circuit simulating an isothermal junction is required. For a chromel-alumel thermocouple the output is approximately 4 millivolt per 100 °C temperature difference.

A DC amplifier having typically a gain of about 100 and a cold junction compensating circuit are required. The latter may readily be realized with the aid of a bridge circuit containing a temperature sensitive resistance.

In order to make measurements to the accuracy required of the digital recording system very accurate and repeatable transducers are required. These are not readily available and hence very careful selection is required. Similarly the accuracy of the signal conditioning equipment has to be very high for the digital system.

There are a number of relatively small self-contained amplifiers commercially available for use as signal conditioners in an airborne environment. These amplifiers are normally mounted separately in close proximity to their associated transducers. In the accompanying table the main characteristics of some typical amplifiers have been tabulated. Amplifiers Nos. 1 and 2 may be used for general purpose amplification of AC voltage signals such as would be obtained from velocity type transducers. Amplifiers Nos. 3 and 4 are charge amplifiers and hence would be used in conjunction with piezo-electric transducers. Amplifier No. 5 is suitable for use with strain gages and could also be used in conjunction with thermocouple transducers.

It is sometimes more convenient, particularly where a large number of transducers is involved to locate all the signal conditioning amplifiers in a single cabinet. To allow amplifiers to be readily interchanged when transducers are changed a plug-in type construction is preferred. (Self contained amplifiers of the type referred to in the previous paragraph cannot be conveniently interchanged if mounted in a single cabinet.) The power supply requirements for a range of amplifiers can usually be rationalized to just a few regulated supply rails using the single cabinet construction. To the author's knowledge a suitable range of plug-in type airborne signal conditioning amplifiers is not available commercially. A summary of some of the plug-in amplifiers required as signal conditioners follows on p. 17.

CHARACTERISTICS OF SOME TYPICAL SIGNAL CONDITIONING AMPLIFIERS

Reference No.	1	2	3	4	5
Type	Columbia Model 5203 AC Voltage Amplifier	Ad-Yu Model A102E AC Voltage Amplifier	Gulton Model FT-3512 Charge Amplifier	Endevco Model 2640 Charge Amplifier	CEC Type 1-362-001 DC Amplifier
Input Arrangement	Single Ended	Single Ended	Single Ended	Single Ended	Differential
Output Arrangement	Single Ended	Single Ended	Single Ended	Single Ended	Single Ended
Input Impedance	> 200M shunted by not more than 20pF	100K			> 1M
Gain	Adjustable from 2 to 50	Fixed, 100 or 10 (selectable via a switch)	Adjustable, 2mV/pcmb to 40mV/pcmb	Adjustable, 2mV/pcmb to 20mV/pcmb	125 nominal, adjustable ±10%
Frequency Response	Flat within ±5% 2 Hz to 50 KHz	Flat within ±3db 1 Hz to 5 MHz	Flat within ±2% 5 Hz to 10 KHz	Flat within ±5% 3 Hz to 20 KHz	Flat within 0·1db DC to 2 KHz
Maximum Output Voltage	5 V peak to peak	11·2 V peak to peak	5·2 V peak to peak	2·8 V peak to peak	10 V peak to peak into 10K
Maximum Output Current	0·5 mA peak to peak	0·8 mA peak to peak			±0·5 mA
Output Impedance	100 ohm max.	100 ohm max.		50 ohm	250 ohm max.
Noise Level	4 mV peak to peak referred to the input with the gain set at 50 and the input shunted by 600 pF or greater	6 μV equivalent input noise with input short circuited	20 mV peak to peak at the output at a gain of 40 mV/pcmb	0·019 pcmb. R.M.S. per 100 pF source capacitance (referred to input) or 1·5 mV R.M.S. whichever is greater	Less than 10 mV peak to peak measured at the output with the input short circuited over the band 0·1 Hz to 5 KHz
Total Harmonic Distortion				1% max.	
Common Mode Rejection					Greater than 100db
Output Zero					Drift less than ±10μV referred to input in 8 hrs. at 77°F. Shifts 0·005% of Full Scale per deg. F from 0°F to 200°F. Adjustable ±5% of Full Scale.
Other Outputs					Bridge excitation supply 10 V. This supply is completely isolated.
Power	28 ± 3 V DC at 25 mA	19·6 V at 3 mA Internal battery	28 V DC at 27 mA	28 + 4 − 8 V DC at 20 mA	28 ± 4 V DC at 100 mA

(i) AC amplifiers having single-ended input and variable gain up to approximately 200 for transducers with single-ended output.

(ii) Differential input low drift DC amplifiers for use with strain gages and thermocouples.

(iii) Charge amplifiers for use with piezo-electric transducers.

(iv) Differential input AC amplifiers with phase sensitive demodulators for use with variable reluctance transducers, L.V.D.T.'s and AC excited strain gages.

In addition to amplifiers other equipment such as filters, and in the case of AC excited transducers, precision oscillators are required.

Development of suitable plug-in amplifiers is at present being undertaken at these laboratories.

A3.2. Power Supplies for Signal Conditioning Equipment

In order to amplify low level transducer signals with a minimum of noise and interference considerable care has to be exercised in the selection or design of power sources. It is essential that "earth" currents such as those arising in an aircraft frame do not flow via signal common lines. Currents flowing through the frame of the aircraft are considerable and millivolt drops across the earthing system are quite possible. The single point earthing technique is usually used to prevent voltage drops in the earthing structure from being picked up with the signals.

As a typical example the Ampex Model AR200 airborne analogue tape recorder derives power from the normal aircraft 27·5 V.D.C. supply, the negative side of which is connected to the aircraft frame. Further the Ampex Model AR200 accepts single-ended input signals the common side of which is connected to the recorder case and also to the supply negative. In Fig. 6(a) a block diagram of a typical recording system using this recorder is shown. The signal conditioning equipment derives power from the aircraft supply in such a way as to cause supply currents to flow through the signal common shields between the signal conditioning unit and the electronics unit. Such an arrangement is poor practice and may be obviated if a DC to DC converter is added as illustrated in Fig. 6(b). Apart from the improved earthing arrangement resulting from the latter technique there is the advantage that a number of supply rails either positive or negative, completely isolated from each other if need be, may be readily furnished. For DC amplifiers providing zero volts output under zero signal conditions both positive and negative supply rails are necessary.

The advantages which arise when a DC to DC converter is used may equally be achieved by the use of self-contained batteries. However, batteries are usually bulky and require frequent attention either in relation to charging or replacement. In addition the temperature range over which batteries can be operated is frequently inadequate.

Similarly the appropriate DC supplies may be obtained from the aircraft 115V 400 Hz supply with the aid of a transformer and associated circuits. While such an arrangement is quite feasible in most aircraft, it presents problems if data has to be acquired elsewhere such as on board ships or in the field.

Regulated supplies of various voltages are required throughout the signal conditioning equipment as power sources for amplifiers, strain gages and the like. In the case of the plug-in signal conditioning amplifiers at present under development at these laboratories the selection of supply rail voltages is usually dictated by the requirements of the linear integrated circuits used. Most linear integrated circuits can be accommodated by voltage rails $\pm$5V, $\pm$10V and $\pm$15V. This selection of supply rails is also consistent with the 10V supply usually required for strain gage bridges and by the 5V supply required by many digital integrated circuits.

PART B REQUIREMENTS FOR A HYBRID RECORDING SYSTEM

B1. ANALOGUE RECORD SYSTEM EXTENSIONS

Most manufacturers of instrumentation magnetic tape recorders provide complete recording and replaying facilities for use with the direct recording system. Adjustments are usually provided on the record amplifiers for bias level and amplifier sensitivity, and on the reproduce amplifiers for the shape of the overall record/replay frequency response. The adjustments

required for shaping the frequency response are invariably difficult and time consuming, particularly as the record and replay head characteristics have to be taken into account.

A system of recording speech and a reference frequency on a single direct recording channel has been developed at these laboratories and is described in Sec. B1.1.

Many manufacturers provide complete recording and replaying facilities for use with the wideband (maximum deviation $\pm 40\%$ of carrier frequency) FM system. Adjustments are provided to allow alignment of record and reproduce amplifiers. FM record and reproduce amplifier alignment is usually a very simple procedure. As the record and replay head characteristics have virtually no effect on alignment the record and reproduce amplifiers can be independently aligned. An FM calibration unit, such as the Ampex Model TC-10, may be used to facilitate amplifier alignment.

Improved signal to noise ratios are possible with the FM system of recording by using servo speed control of the tape reproducer machine and by using flutter compensation techniques. Some development along these lines has proceeded at these laboratories and is discussed in Sec. B1.2.

The PDM recording system usually requires fairly complex data acquisition and reduction equipment which are not normally supplied by tape recorder manufacturers. Ampex Corporation, for instance, provides a PDM record amplifier which accepts information already in PDM form and provides suitable record head output. No multiplexing or keying equipment is provided by the above manufacturer. Similarly no de-keying or de-multiplexing equipment is provided on the reproduce side. Some manufacturers of data acquisition and reduction equipment produce keying and de-keying equipment for use with the PDM system. However, PDM systems frequently require to be adapted to the particular needs of the user, a factor which makes standardization of equipment difficult.

In Sec. B1.3 the PDM system requirements are analysed and lines of future expansion are indicated. In particular the use of digital computer techniques for reduction purposes is considered.

B1.1. Recording of Reference Frequencies

The recording of appropriate reference frequencies is required for the following reasons:

(i) To check the speed stability of the recorder tape transport.

(ii) To enable servo speed control and flutter compensation to be incorporated on replay.

Reference frequencies as specified by IRIG[16] are usually adopted. These frequencies are generally used by manufacturers of analogue tape reproducers fitted with a fast response servo speed control. The frequencies are tabulated below.

Tape Speed	Compensation Tone Frequency
60 ips	100 KHz
30 ips	50 KHz
15 ips	25 KHz
$7\frac{1}{2}$ ips	12·5 KHz
$3\frac{3}{4}$ ips	6·25 KHz
$1\frac{7}{8}$ ips	3·125 KHz

The reference frequency stability as laid down by IRIG is required to be better than $0{\cdot}01\%$. To achieve such stability a crystal oscillator is required.

In a recording system which has been developed at these laboratories the reference frequencies tabulated above have been adopted. Further, clock signals for a digital data acquisition system at present under development (Sec. B2) are also required. It is intended that these clock frequencies also be derived from the same crystal oscillator providing the reference frequencies.

So that one record channel need not be completely taken up for the recording of reference frequencies it is desirable that speech and reference tones be recorded on a single direct record track. Card[28] has developed a crystal oscillator and suitable dividing circuits to obtain the

required reference frequencies. Further, using a balanced modulator, he records both reference frequency and speech on a single direct record track. A block diagram of the arrangement used for the recording is given in Fig. 7.

On replay the composite signal is passed through a zero crossing detector to provide the reference frequency output. The speech is separated using a suitable demodulator. The replay arrangement is depicted in block form in Fig. 8.

B1.2. Improvement in Signal to Noise Ratio in the FM Recording System

The accuracy of an FM recording system is largely dependent on the speed stability of both the record and the replay machines. Long term speed shifts between record and replay give rise to DC errors in the demodulated output. Alternating speed variations between record and replay give rise to an unwanted AC component or noise in the demodulated output. Athey[29] discusses the various causes which give rise to disturbances in tape motion and hence speed irregularities. Careful design of the tape transports greatly reduces these unwanted speed variations.

Further improvement in the signal to noise ratio is possible using a servo speed control on replay. Such a system requires the recording of a stable reference frequency as described in Sec. B2.1. Assuming that the reference frequency is absolutely stable then any frequency changes appearing on replay will be due to speed variations between record and replay (neglecting any tape elongation or shrinkage between record and replay). Some years ago servo speed control was used only for maintaining the average replay speed equal to that for record. The standard practice was to record a 17 KHz or 18·24KHz carrier modulated by the 60 Hz (or other frequency) used to drive the capstan on record. On replay the 60 Hz signal was demodulated and used to control the frequency of the power source driving the reproduce capstan. More recently servos with a higher degree of sophistication have been introduced. These servos control the instantaneous rather than the average speed. Usually a 100 KHz signal or sub-multiple thereof is recorded to constitute the reference. Ampex Corporation provide such a system in their Model FR 1260 Recorder/Reproducer.

It is also possible to use the recorded reference frequency in a "flutter compensation" system. In such a system, compensation is applied by electronic circuits to reduce the effects of speed variations on the outputs of the FM reproduce channels. There are many problems associated with flutter compensation. To obtain an improved signal to noise ratio it is essential that the channel which is to be compensated is subject to exactly the same speed disturbances with regard to both amplitude and phase as the channel on which the reference frequency is recorded. The staggering of analogue heads makes this very difficult to achieve if the two channels in question belong to different head stacks. At the higher frequencies phase differences in the flutter even across the width of the tape can render the compensation useless.

Some work has been done by Card[28] on a flutter compensation system which changes the area of the pulse appearing in the FM discriminator in sympathy with the variations in the reference signal frequency. The flutter compensation system is depicted in Fig. 9. Further work is required to ascertain whether any appreciable improvement occurs using flutter compensation in addition to the instantaneous servo speed control.

B1.3. PDM System Requirements

No multiplexing, de-keying or de-multiplexing equipment is presently available at these laboratories for use in the PDM system of recording.

Airborne PDM keyers are available at these laboratories for use in the PDM system of recording. The dynamic range of these keyers is variable from 310 to 610 microsecond and the minimum pulse duration from 60 to 170 microsecond. Ampex Corporation provides plug-in PDM record amplifiers which accept the PDM output from the above keyers and produce suitable drive currents for the record head fitted to their Model AR200 airborne tape recorder. Amplifiers of this type are available at these laboratories.

The precision with which the pulse durations can be recorded and reproduced is a function of tape speed. Some tests are required to provide this information.

In Fig. 10 a block schema of a typical PDM recording system is illustrated. For a detailed description of a PDM recording system refer to Sec. A1.4. The signal level range required at the input of the keyer is typically 0 to 5 volts. Hence for many measurements pre-amplification

of signals is required. Signal pre-amplification may be performed either before or after the multiplexer. If pre-amplification is performed prior to the signals reaching the multiplexer then separate pre-amplifiers are required on each data channel. While this system is quite expensive because of the large amount of signal conditioning equipment required it has the advantage that the demands on the multiplexer are minimized. To achieve the 900 per second keying rate (as laid down by IRIG[16]) a solid state multiplexer is required. For high level multiplexing a single ended arrangement is adequate. If pre-amplification is performed after the multiplexer, a low level differential type of multiplexer is required. Very stringent accuracy requirements are placed on such a multiplexer particularly in view of the relatively large temperature range over which the equipment must perform. For more details on multiplexers refer to Sec. B2.4.1. It is envisaged that a 20 channel system will be adopted originally.

In order to identify each channel on replay it is essential that some form of synchronizing signal be recorded. One method of providing the synchronizing information is to provide one pulse (per complete scan of the multiplexer) with a duration greater than that given by 100% signal (say 5·5V for synchronizing pulse as compared with 5·0V for 100% signal). For such a system it is essential that the signal channels are prevented from exceeding 100% level. Another system of providing the synchronizing information is to completely eliminate one pulse per complete scan of the multiplexer. This may be achieved by preventing the last clock pulse (say) from reaching the keyer. This latter system overcomes the difficulty, inherent in the previous system, of ensuring that 100% signal is not exceeded on any of the signal channels.

A signal channel reading zero volts must produce a finite pulse width. In the case of the airborne PDM keyers available at these laboratories the pulse duration corresponding to zero volts is adjustable from 60 to 170 microsecond.

Calibration signals representing 0% and 100% level are very desirable and should be connected to two of the inputs of the multiplexer. These signals allow calibration of the data signals on replay.

The proposed timing of the PDM record system is illustrated in the table below.

Period per sample (At 900 per second)	1111 microsecond
Minimum pulse duration (Corresponding to 0V)	100 microsecond
Maximum pulse duration (Corresponding to 5V or 100% signal)	600 microsecond
Dynamic range	500 microsecond
Minimum time from end of pulse to beginning of next	511 microsecond

Reconstruction of the PDM waveform may be performed on replay using a suitable reproducer. An Ampex Model FR1200 Recorder/Reproducer is at present available at these laboratories for this purpose.

Two main decoding systems for the PDM data will be considered, one which is self contained and one which requires the use of a digital computer.

In Fig. 11 a block schema of a proposed decoding system which does not require the use of the digital computer has been drawn.

One simple method of detecting the synchronizing pulse is to use a ramp generator which is switched on during the "pulse absent" periods for the "pulse absent" method of synchronization or switched on during the "pulse present" periods for the method of synchronization which employs a pulse of longer duration than that corresponding to 100% signal. In each case the longest period will occur when the synchronizing signal arrives. With the addition of a voltage comparator a synchronizing pulse is generated which is used to reset the sequence generator.

The multiplexed PDM signal is taken off to an oscillator which free runs with a slightly longer period than the sample period. In this way pulses for the sequence generator are generated even if a tape drop-out occurs during a complete sample. Hence the system becomes fairly immune (as regards de-synchronization) to spurious pulses. The output of the oscillator provides clock pulses for the sequence generator which provides gate pulses for each output in turn. If a 20 channel system is used the sequence generator will contain a count by 20 circuit which ideally requires only one synchronizing pulse per record to set the counter correctly. Hence if for some reason a synchronizing pulse is missed the system will still remain in synchronism. Synchronizing pulses subsequent to the first merely check that the sequence generator is correctly set.

The multiplexed PDM signal and the outputs from the sequence generator are passed through "AND" circuits to separate individual channels. The oscillator, the sequence generator and the "AND" circuits constitute a de-multiplexer.

The outputs from the de-multiplexer are in PDM form and require demodulation by means of a de-keyer. Fig. 11 indicates one possible method in which the PDM signals gate time interval counters. A digital output may be made readily available from the counters. If an analogue output is required a digital to analogue converter is required in conjunction with the counters. If the data is decoded one channel at a time one counter and one digital to analogue converter would suffice.

In the second system of decoding the PDM data a digital computer may be used with suitable peripheral equipment. An electronic counter which is capable of measuring pulse durations with up to at least 1 microsecond resolution and which has a suitable digital output could be used for demodulating the PDM data and providing a suitable interface for a digital computer. The Model 5245M Electronic Counter of Hewlett Packard manufacture is one counter which would meet the requirements. It will provide up to 0·1 microsecond resolution and has a suitable digital output. To accommodate keying rates up to 900 per second the counter storage time must be fairly low (in the order of 500 microseconds maximum assuming 600 microseconds is the maximum pulse duration used). Normally the Model 5245M stores the display for at least 200 millisecond before another measurement can be made. However, the manufacturers state that this counter can be readily modified to accommodate 900 readings per second in the range 100 to 600 microseconds.

The de-multiplexing function may be performed by the digital computer with the aid of a suitable programme.

Channel identification presents some problems. A marker pulse which has a pulse duration longer than the pulse duration equivalent to 100% signal could be easily identified. However, if a pulse is omitted once per multiplexer sequence to provide synchronizing information additional circuits would be required.

B2. PROPOSAL FOR A DIGITAL RECORDING SYSTEM

As stated in Sec. A2 a PCM (or digital) system of recording is required to enable recording of some flight parameters to an accuracy of 0·1% approximately.

In aircraft studies a need exists for the simultaneous recording of analogue and digital information. For example, time correlation between Mach Number (calculated from a number of highly accurate measurements which must be recorded using digital techniques) and a vibration level (which must be recorded using wideband analogue techniques) may be required.

In the following sections a digital recording system meeting the above requirements is proposed and analysed.

B2.1. Tape Recorder Requirements

As indicated in the Introduction the use of separate tape machines for simultaneous analogue and digital recording is not practical for investigations involving smaller aircraft. A hybrid system in which analogue data and digital data are recorded on the same tape is preferred.

In analogue recorders two separate headstacks incorporating alternate tracks are required to obtain satisfactory performance with respect to crosstalk. In digital recorders crosstalk is not a significant problem and all tracks are situated on a single headstack. Further the heads used in analogue recorders generally have inferior skew characteristics when compared with

digital record heads. Hence high speed parallel digital recording is generally not possible on an analogue recorder. However, the above limitations in relation to analogue recorders are no longer significant for serial digital recording on a single track.

For a given tape speed a single channel digital recording system cannot cope with information rates as high as can be handled by a parallel system. Fortunately the bandwidth requirement for most aircraft parameters which must be recorded using digital techniques is usually moderately low (Sec. A2) and in such cases the restriction on information rate can be tolerated.

In order to check the recorded digital information and provide some degree of immunity against errors due to tape drop-outs the recording of lateral parity checkbits is essential. For this reason it is proposed that serial digital data be recorded on one track and lateral odd parity checkbits on another track. The two tracks to be chosen for the digital recording must be situated on the same headstack and preferably close to the centre of the tape to minimize skew. For a seven channel recorder tracks 3 and 5 would be a suitable choice. Although the recording of a parity track effectively constitutes a form of parallel recording with the associated demand for low skew the problem is not nearly as great as with seven track parallel digital recording. Steer[30] discusses a similar system of recording.

In the proposed system a seven channel Ampex Model AR 200 airborne analogue magnetic tape recorder (available at these laboratories) is to be used for recording analogue data on tracks 1, 2, 4, 6 and 7 and for recording digital data and parity on tracks 3 and 5.

A NRZM (also called NRZI) type of recording is to be adopted. This type of recording is the one most commonly used. Fairly high data packing densities and fairly good immunity from drop-outs can be achieved using the NRZI technique (Sec. A1.5).

It is envisaged that occasionally when large quantities of digital information only have to be recorded a full seven channel digital recording system may be desirable. Ampex Corporation provide a seven track IBM compatible write head and plug-in digital record amplifiers for use with the Model AR 200. Since the Model AR 200 is basically an analogue machine special guiding (a standard modification performed by Ampex Corporation) is required to provide a workable seven track digital recording system. With the above additions the AR 200 digital system can accommodate a maximum bit packing density of 500 bits per inch, compared with the standard IBM packing densities of 556 bpi or 800 bpi.

The digital record amplifiers, which may be inserted directly into any standard AR 200 Record Electronics Cabinet, do not provide write deskew and hence adjustable deskew networks would be required on replay to enable the maximum specified bit packing density to be attained. These amplifiers accept digital data in the appropriate NRZ form and provide the necessary record currents for the write head.

The modified AR 200 machine is, of course, still a continuous recording device and lacks the fast start/stop capability usual in digital recorders.

To summarize, a hybrid recording system, using two channels of an analogue tape machine for digital recording and the remaining channels for analogue recording, is proposed for use in aircraft studies. Further, for the occasions when large quantities of digital information only have to be recorded, a seven channel parallel digital recording system which utilises the same analogue machine as used for the hybrid system is suggested.

B2.2. Digital Data Acquisition Equipment Requirements

It is essential that the digital section of the data acquisition equipment be capable of accepting input data which originates in either analogue or digital form.

Analogue data, such as the outputs from high precision transducers, requires conversion to digital form. Initially up to 16 analogue input channels are to be accommodated. However, the ability to expand this number at a future date is highly desirable. An overall accuracy of 0·1% (Sec. A2) is required. A maximum sample rate of 50 per second for each channel meets most requirements. To achieve the maximum sampling rate the Ampex Model AR 200 could be run at its maximum speed of 60 ips. For lower tape speeds it is envisaged that the sample rate will be made proportionately lower.

Since the voltage levels of the input analogue data may vary considerably it is essential that the data acquisition equipment accept a wide range of input levels.

Digital input data relating to run number (fixed throughout any particular run) and time of day information must also be accepted by the digital data acquisition equipment. Since this digital input data is in parallel form a parallel to serial conversion is required.

B2.3. Proposed Record Format

In order to accommodate the wide range of analogue input levels, it has been decided that a suitable multiplexer together with an anlogue to digital converter having an auto ranging facility be used. The auto ranging facility virtually eliminates the need for signal conditioning amplifiers associated with each analogue input. Dynamics Systems Electronics Corporation offers an airborne ADC having 11 signal ranges in binary steps from ± 10 mV to $\pm 10{\cdot}24$ V. Range changing may be auto (at the expense of reduced conversion speed) or programmed. In the auto range mode of operation the ADC is ranged with the input signal scaled to no less than the upper 47% of the lowest possible range. The dynamic range of the airborne ADC offered by Dynamics Systems Electronics Corporation fits the present needs very closely. Range is identified by a 4 bit word.

To achieve the overall accuracy of $\pm 0{\cdot}1\%$ of full scale a resolution of at least 1 part in 1000 is required. To allow for other errors the resolution, expressed as a percentage of full scale, should be somewhat better than the overall accuracy figure. A resolution of 1 part in 2047 ($2047 = 2^{11} - 1$) of full scale should suffice. Assuming that the magnitude is expressed in pure binary code 11 bits will be required. Since the input signals may be of either polarity an additional bit is required to represent sign. A 2's complement format is illustrated an Fig. 12 is required.

Bits for word address identification are not required since the sampling sequence will remain invariant during any series of tests. By counting from the synchronizing word (to be discussed later in this section) separate channels may be readily identified.

Apart from the lateral parity checkbits to be generated for each data bit a longitudinal parity checkbit at the end of each word is also desirable. In order to meet both lateral and longitudinal parity requirements an additional "dummy" bit is required (Sec. B2.4.4).

Spaces are required to separate words. A space of 2 bit positions should be adequate. Under these conditions a word and associated gap would occupy 20 bit positions composed of 12 bits to represent magnitude and sign of the measured quantity in 2's complement format, 4 bits to represent range (or multiplier), 1 bit for the "dummy," 1 bit for the longitudinal parity check character and 2 bit spaces for the interword gap.

It is desirable that the words used to represent the digital input information (composed of run number and time of day information) be made similar to the data words corresponding to the analogue input information. Hence these words should be composed of 16 information bits, 1 "dummy" bit, 1 longitudinal parity checkbit and 2 bit spaces corresponding to the interword gap. If the information bits are less than 16 the difference can be made up by adding zeros.

Both run identification and time of day require appropriate encoding by the digital data acquisition equipment.

The run number could readily be set up by means of digital switches having appropriate parallel digital output. If a run number range of 0000 to 9999 is employed and each decimal digit is encoded using 1–2–4–8 BCD code, then a total of 16 bits will be required.

The proposed arrangement utilizes preset switches to provide month-of-the-year and day-of-the-month information, and a time of day generator to provide time of day with 1 second resolution. The table below indicates the format which has been chosen.

Time Information			Format Details
Type of Data	Units	Measurement Range	Digital Output
Preset	Month	1 to 12	5 bits 1–2–4–8 BCD
	Day	1 to 31	6 bits 1–2–4–8 BCD
Variable	Hours	0 to 23	6 bits 1–2–4–8 BCD
	Minutes	0 to 59	7 bits 1–2–4–8 BCD
	Seconds	0 to 59	7 bits 1–2–4–8 BCD

A total of 31 bits is required. One zero may be added to make two 16 bit words.

It is proposed that a gap corresponding to one complete word be recorded to provide synchronizing information. The above gap would be inserted once per complete frame of data (i.e. after each input has been sampled once) for identification of channels. The complete frame of data will be referred to as a "RECORD" and the gap corresponding to the synchronizing word will be referred to as an "INTER-RECORD GAP." Allowing 16 words for the sampled analogue data, 3 for the sampled digital data and 1 for synchronization gives a 20-word record. It is desirable that the number of sampled analogue signals be variable up to the maximum number of 16. Suitable programmer design will enable this to be readily achieved. Hence the maximum record length will be 20 words or 400 bit positions, allowing 20 bit positions per word.

To achieve the required sampling rate of 50 per second (Sec. B3.2) for each channel a record rate of 50 records per second is required. The corresponding bit rate is 50 $\times$ 400 bits/sec or 20 K bit/sec. The maximum recording rate is possible at 60 ips tape speed. Corresponding lower rates are obtainable at lower tape speeds as indicated in the following table.

Tape Speed	Bit Rate	Word Rate	Record Rate*
60 ips	20 K bit/sec	1000 word/sec	50 Record/sec
30 ips	10 K bit/sec	500 word/sec	25 Record/sec
15 ips	5 K bit/sec	250 word/sec	12·5 Record/sec
$7\frac{1}{2}$ ips	2·5 K bit/sec	125 word/sec	6·25 Record/sec
$3\frac{3}{4}$ ips	1·25 K bit/sec	62·5 word/sec	3·125 Record/sec
$1\frac{7}{8}$ ips	625 bit/sec	31·25 word/sec	1·5625 Record/sec

* For maximum record length of 20 words.

For each operating speed indicated in the above table the information packing density on the tape remains invariant at $333\frac{1}{3}$ bpi.

In Fig. 13 details of the word and record formats are given, including lateral parity bits (odd) and longitudinal parity bits (even).

B2.4. System Detail

A block schema of the proposed digital data acquisition system is given in Fig. 14. The various units of equipment which make up the digital data acquisition equipment will now be analysed in detail.

B2.4.1. Multiplexer

To achieve a word rate of 1000 words per second (the maximum required—see Sec. B2.3) the multiplexer must be capable of a switching rate of at least 1000 channels per second. A solid state multiplexer must be used to realize such a high rate of switching.

Input levels ranging from 10 mV full scale to 10·24V full scale have to be handled by the multiplexer (Sec. B2.3). To accommodate the low level signals a differential type multiplexer (both input lines individually switched) is required.

In recent years FET type switches have been used extensively in multiplexer applications. These switches, with zero offset voltage, do not suffer from the difficulties with conventional transistor switches (e.g. Bright switch) in which the offset voltage is temperature dependent. Very high input impedance, typically 100 megohm, can be achieved with FET switches in the "off" condition. The series "on" resistance is, however, four to five times greater than that of conventional transistor type switches. By using a suitable buffer amplifier the effect of the "on" resistance can be made quite negligible. Loading of the transducer or other signal source is also prevented by using a suitable buffer amplifier.

One of the most important characteristics required of the multiplexer switch is high common mode rejection. The presence of high common mode signals is likely in many measurement applications. A common mode rejection ratio of the order of 120 db is required at DC and at least 60 db at 400 hertz (allowing up to 100 ohms source unbalance). To obtain such values of common mode rejection very specialized circuit techniques are required.

In Fig. 15 a generalized input arrangement is drawn. Z_1 and Z_2 are the signal source impedances; Z_3 and Z_4 are the impedances to ground from each of the differential inputs. V_{CM} and V_D are the common mode input and the differential input respectively. Portion of the common mode signal, V_{CM}, produces a differential input to the amplifier. Let V_C equal the voltage applied differentially to the input by virtue of V_{CM}. From Fig. 15 we may write:

$$V_C = V_{CM}\left(\frac{Z_2}{Z_2 + Z_4} - \frac{Z_1}{Z_1 + Z_3}\right)$$

$$\frac{V_C}{V_{CM}} = \frac{Z_2}{Z_2 + Z_4} - \frac{Z_1}{Z_1 + Z_3}$$

The above ratio V_C/V_{CM} must exceed 10^6 to 1 to achieve 120 db common mode rejection. Theoretically the ratio is infinite if there is a perfect balance of the inputs (i.e. $Z_4/Z_2 = Z_3/Z_1$). Such perfect balance is difficult to approach unless an input balance adjustment is incorporated. In a multiplexer where a number of different inputs are switched sequentially to the input of the amplifier (referred to earlier as a "buffer amplifier") it is not feasible to have a balance adjustment at the input.

If the impedances to ground are equal ($Z_3 = Z_4$) and much larger than the source impedance (Z_1 and Z_2) then:

$$\frac{V_C}{V_{CM}} = \frac{Z_2 - Z_1}{Z_3}$$

If there is 100 ohm unbalance in the source impedances (i.e. $Z_2 - Z_1 = 100$ ohm) then to achieve 120 db common mode rejection:

$$Z_3 = Z_4 = 10^6(Z_2 - Z_1)$$

$$= 10^6 \times 100 \text{ ohm}$$

$$= 100 \text{ megohm}$$

The above resistance values for Z_3 and Z_4 would suffice (assuming 100 ohm source unbalance) if there were no other impedances involved. However, cable and other capacitances normally appear as shunt impedances at the input to the amplifier (effectively shunting R_3 and R_4, the resistance components of Z_3 and Z_4 respectively). In such cases the common mode rejection ratio would fall off markedly with frequency. The problem can be greatly alleviated if an additional common mode amplifier, which senses the magnitude of the common mode voltages and drives the capacitance of the shields, etc., is used. The amplifier arrangement is depicted in Fig. 16.

The common mode amplifier must have a high input impedance to avoid shunt effects on Z_4. The gain must be close to unity and the response must be fast in order to drive the capacitances at a high slewing rate.

Dynamics Systems Electronics Corporation offers airborne multiplexers incorporating the amplifier arrangement of the type depicted in Fig. 16. One of the range of airborne multiplexers offered by the above manufacturer meets the requirements laid down in this Section. It has the following specification:

1. Accuracy	±0·05%
2. Input	
(a) Arrangement	Two wire differential, shielded
(b) Level	±10 mV to ±10·24 V
(c) Impedance	The differential "on" impedance is 10 megohm (min.) and the differential "off" impedance is 100 megohm (min.). The common mode impedance is 1000 megohm (min.) resistive in shunt with 100 picofarad (max.) capacitive.

3. Common Mode Rejection	120 db at D.C. 100 db at 60 Hz
4. Source Unbalance (maximum allowable unbalance for specification to apply)	100 ohms
5. Crosstalk	$\pm 0{\cdot}02\%$ (max.)
6. Output	
(a) Voltage	± 10 V
(b) Current	10 mA (max.
(c) Output Impedance	1 ohm (max.)

The multiplexer switches offered by Dynamics Systems Electronics Corporation are organized into groups of 5. The output of each switch in the group is connected to a common signal bus. Signal buses corresponding to each group of 5 switches are in turn switched via a group switch which will accept 5 inputs also. The switching pattern is continued such that no group switching unit has more than 5 inputs connected to it.

Control of a multiplexer of the type offered by Dynamics Systems Electronics Corporation is provided by the programmer which is discussed in detail in Sec. B2.4.5.

Switching rates in the vicinity of 200 channels per second are feasible using reed relay switches. However, it is to be remembered that like all mechanical type switches the life of the switch is limited and becomes an important consideration when high switching rates are employed. Reed relay switches can readily be made 3-way for switching 2 signal leads plus a shield. Using special design techniques these switches can be made with low thermal offset voltages and low noise. In view of these properties the reed relay switch is suitable for relatively low level switching applications. Cost and circuit complexity for the reed relay type switch are much reduced when compared with the solid state switch. The limitations with respect to switching rate make the reed relay type switch unsuitable for use at the higher switching rates required of the multiplexer discussed in this section.

The requirements of the multiplexer to be incorporated in the digital data acquisition equipment are similar to those of the PDM multiplexer (Sec. B1.3). It is intended that the multiplexer be readily separable from the remainder of the digital data acquisition equipment to that it can also be used in conjunction with the PDM system.

B2.4.2. Analogue to Digital Converter

There is quite a range of methods employed to perform analogue to digital conversion, some of which are discussed by Digital Equipment Corporation.[31] Most commercially available analogue to digital converters (abbreviated ADC) are of the "counting" type or the "weighing" type.

In the counting type of converter a number of pulses proportional to the analogue voltage being measured is gated into a counter. The digital output from the counter at the completion of the count is a measure of the analogue input. The counters may be readily arranged to provide BCD output if required.

One method of providing a count proportional to the analogue input uses a constant repetition rate pulse input, a digital to analogue converter (abbreviated DAC) associated with the counter and a voltage comparator. The analogue output from the DAC is compared with the analogue input. When coincidence occurs the counting is stopped and the count registered in the counter is a measure of the analogue input. For this type of ADC the conversion time will depend on the input level.

Another method of providing a count proportional to the analogue input uses a voltage to frequency converter in which counting of the output is performed over a constant time interval. This method is frequently used in integrating type ADC's where usually the counting time interval is made an integral number of power line cycles. Such ADC's have high noise rejection characteristics, including interference at power line frequencies.

In the weighing type of converter a successive approximation technique, in which the voltage range is repeatedly divided in half, is usually used. A simplified diagram of a successive approximation converter is drawn in Fig. 17. Each flip flop in the output register is successively

set to the "1" state. The output of the DAC is compared with the analogue input. If the DAC output is greater than the analogue input the flip flop which was last set to the "1" state is reset to the "0" state on the next clock pulse, but if the DAC output is less than the analogue input the flip flop remains set. Bits are generated serially at regular intervals in synchronism with the clock pulses with the most significant first and the least significant last. The conversion time of the successive approximation ADC is proportional to the number of bits. By virtue of the manner in which the conversion is performed the successive approximation converter lends itself most readily to a pure binary representation of the magnitude of the voltage being measured.

For counting type ADC's the conversion time is doubled for every additional bit required and hence considerable conversion time may be required in high resolution systems. To obtain a resolution of 1 part in 2047 at 1000 per second conversion rate requires a frequency in excess of 2·047 MHz. If auto ranging is also required the frequency will probably need to be increased at least by a factor of 2, say to 5 MHz to allow a small margin. Of the counting type converters discussed the one employing a voltage to frequency converter is attractive because of the high noise rejection characteristics. However, it is to be remembered that as the conversion time would need to be less than 1 millisecond only high frequency noise (above 2 KHz) would tend to be reduced by the integration process. Since a good deal of aircraft noise is below 2 KHz it is questionable whether the integration would provide any great advantage. To provide the required resolution, operation speed, and the auto ranging facility the voltage to frequency converter would need to operate with a maximum frequency of about 5 MHz. While such converters would seem practical the author is unaware of any supplier of an airborne ADC of this type.

The successive approximation converter, while it may not be quite as good as the integrating type with regard to noise rejection, easily provides the conversion speed and the resolution required. Since airborne ADC's of the successive approximation type are commercially available it is envisaged that this type of converter will be used.

Auto ranging in binary steps from ± 10 mV to $\pm 10{\cdot}24$V (Sec. B2.3) is required. In addition it must be possible to operate in a programmed range mode in which any of the above ranges can be chosen. Representation of the range is required to be in 4 bits (pure binary).

The inputs to the ADC may be of either polarity. Sign is to be represented in a 2's complement format.

A resolution of 1 part in 2047 ($2047 = 2^{11} - 1$) is required which is obtainable using 11 bits. The 2's complement format increases this number to 12. Allowing 4 bits for range indication means that a 16 bit output is required from the ADC.

Timing and run number information are inherently in digital form (Sec. B2.3) and hence parallel to serial conversion of this data is essential prior to recording. Both serial and parallel outputs are readily available from the successive approximation ADC. Since a parallel to serial converter has to be provided it is convenient to utilize only the parallel output from the ADC.

Internal clocking of the ADC is quite acceptable provided that the conversion is always complete within less than 1 millisecond. External clocking can be used to provide appropriate serial data transfer to the tape.

To allow the multiplexer to be switched while conversion is taking place it is essential that a "sample and hold" circuit be incorporated at the front end of the ADC. The sample time must be small compared with 1 millisecond, say 100 microseconds or less.

Dynamics Systems Electronics Corporation offers an airborne successive approximation ADC which meets the requirements. A summary of the specification for this ADC follows:

1. Analogue Input

1.1. Signal Ranges	11 ranges in binary steps from ± 10 mV full scale to $\pm 10{\cdot}24$V full scale are provided.
1.2. Range Determination	The signal ranges are: (i) Externally programmable. (ii) Automatically ranged with the signal scaled to no less than the upper 47% of the lowest possible range.
1.3. Polarity Determination	The polarity is determined automatically.
1.4. Input	The input is differential and the input impedance is less than 10 megohms at D.C.

2. Sample and Hold Feature	An analogue signal sample and hold circuit is incorporated. If required this circuit can be disabled. In the programmed range mode of operation the sample is complete within 1 microsecond after the "conversion trigger" (See 4.3).
3. Digital Output	
3.1. Magnitude	The magnitude and sign is expressed as a 12 bit pure binary word in 2's complement format.
3.2. Range	The range is expressed as a 4 bit word.
3.3. End of Conversion	An output signal indication that the conversion is complete is provided.
4. Digital Inputs	
4.1. Ranging Select	Program or auto range operating modes are selectable via the logic state of one input line.
4.2. Range	In the programmed range mode of operation a 4 bit input word selects the appropriate range.
4.3. Conversion Trigger	The conversion process is initiated by the leading edge of a command to convert signal appearing on one input line.
5. Conversion Speed	In the auto range mode of operation the conversion is complete within 900 microseconds after the leading edge of the conversion trigger. In the programmed range mode of operation the conversion is complete within 500 microseconds after the conversion trigger.
6. Resolution	Full scale is represented by $2^{11} - 1$. Hence a resolution of 1 part in 2047 is obtainable.

B2.4.3. Digital Clock

A digital clock having 1 second resolution is required to enable recording of a real time scale on the tape. The recorded time scale will allow:

(i) A real time scale to be put on graphs or results on replay.

(ii) Data on different tracks obtained from a given tape during different replay runs to be accurately associated in time.

(iii) A means of identifying and locating any regions of special interest on the tape.

Usually analogue records requiring a real time scale utilize the output of a Time Code Generator on one track. Time codes produced by Time Code Generators are usually one of several standard codes. In most cases the time code consists of a sinusoidal carrier (usually 1 KHz) amplitude modulated by a serial digital type signal. Since a digital recording is to be provided for the data acquisition equipment under consideration it is logical to record the time information with the rest of the digital information. For this purpose a Digital Clock having a parallel digital output is adequate. The Time Code Generator is considerably more complex as a parallel to serial converter and a modulator are also required.

The output of the Digital Clock is to be in hours, minutes and seconds using BCD 1-2-4-8 code, "1" state positive. The requisite number of bits is indicated in the table below.

Unit	Range	Number of Bits Required
Second	0 to 59	7
Minute	0 to 59	7
Hour	0 to 23	6

Hence a total of 20 bits is required to give time of day in BCD format.

Timing pulses are to be derived from the crystal oscillator used to provide reference and clock frequencies (Sec. B1.1). Frequency division to obtain 1 Hz pulses is the first requirement of the Digital Clock. This may readily be obtained using 4 decade dividers in conjunction with the 10 KHz clock frequency required by the digital data acquisition equipment (Fig. 7).

An in-line display of time of day in hours, minutes and seconds is required and is easy to arrange if BCD is used. Hence BCD is chosen in preference to pure binary code although slightly more bits are required.

Other digital information preset by decimal thumbwheel switches on the front panel is to be provided. The month of the year and the day of the month are to be settable by decimal switches. These switches must provide a BCD 1-2-4-8 output code. The day of the month is to be settable anywhere between 1 and 31 and hence requires 6 BCD bits, the month of the year is to be settable anywhere between 1 and 12 and hence requires 5 BCD bits, and thus a total of 11 bits is required.

Adding the above number of fixed data bits to the 20 bits already required for time of day information gives a total of 31 bits. Hence two 16 bit words will suffice for time and date information. A zero may be recorded for the 32nd bit not required.

The Digital Clock is also to incorporate means for setting the run number which will remain invariant for any run. Four decimal digits (in the range 0000-9999), requiring a 16 bit word for 1-2-4-8 BCD representation, will be allocated for run number which will be settable using thumbwheel switches and will normally be coded in the form 37-69 meaning Run No. 37 for 1969.

Start and stop pushbuttons are to be provided for starting and stopping the clock. A reset pushbutton is to be provided for resetting all the flip flops to zero (to give "0" time).

Depressing a "Time Set" pushbutton must set the timing flip flops to a time preset by 6 decimal switches on the front panel and also start the timing.

The accuracy required of the Digital Clock is ± 1 second per day over the temperature range $-55\,^{\circ}C$ to $+95\,^{\circ}C$ and the complete environment of MIL-E-5400 for Class 3 operation.

The Digital Clock is to be powered from aircraft 28 V DC supply but isolation between supply common and the output common must be provided (a DC to DC converter is envisaged).

The Digital Clock, a block diagram of which is given in Fig. 18, is currently under development at these laboratories.

B2.4.4. Output Format Generator

The requirements for an output format generator to be developed at these laboratories are analysed in this section. Both serial and parallel outputs (Fig. 14) are required.

For the basic "serial output," two channels of digital information, a data channel and a parity channel, are required. Each channel is to provide serial digital information in NRZI form (Sec. B2.1). Since the input data from the Analogue to Digital Converter and the Digital Clock is in parallel form, parallel to serial conversion is necessary. The Output Format Generator is required to provide a suitable serial output and to generate the requisite parity bits.

In the alternative case of the seven channel digital recording (Sec. B2.1 and Fig. 14) which may at times be required it will be necessary to provide a seven channel parallel digital output. The seven channel output will consist of six data channels and one lateral parity channel. The circuits associated with the "parallel output" will be discussed in the latter part of this section.

Most of the circuits required for the Output Format Generator (and also for the Programmer discussed in Sec. B2.4.5) can be readily developed using commercially available digital integrated circuits as "building blocks." There is a range of logic types available on the semiconductor market such as RTL (Resistor Transistor Logic), DTL (Diode-Transistor Logic), TTL (Transistor-Transistor Logic) and various combinations of these types. It has been decided that a TTL type be used as it provides better output drive capability and lower susceptibility to capacitively-coupled noise than either RTL or DTL, and is capable of very fast operation.

The Texas Instruments Series 54 TTL integrated circuits designed to operate over the temperature range $-55\,^{\circ}C$ to $+125\,^{\circ}C$ meet all the requirements. In Fig. 19 the logic symbols to be used in this paper are defined.

If the 16 bit input words (from the Analogue to Digital Converter and the Digital Clock) are entered in parallel into a 16 bit shift register then a serial output can be readily produced by shifting the pattern through the register. The circuit of Fig. 20 has been devised to provide an appropriate serial output. Control signals for the Output Format Generator are provided by the Programmer (to be discussed in Sec. B2.4.5).

Each word which appears at the output of the Output Format Generator is composed of 16 information bits, 1 "dummy" bit, 1 longitudinal parity checkbit and 2 bit spaces (Sec. B2.3) and hence has a duation equal to that of 20 bits. The period of each word can be divided up

into 20 equal time intervals associated with each bit which we will designate B0 to B19. In a logic context the symbol B9 (for instance) means that B9 is a quantity which takes on a "true" or logical one value during the time interval associated with B9 and takes on a false or logical zero value at all other times.

The bit rate is equal to the frequency of the incoming clock signal which is derived from the crystal oscillator referred to in Sec. B1.1. The frequency of the clock signal varies from 625 Hz (maximum for $1\frac{7}{8}$ ips tape speed) to 20 KHz (maximum for 60 ips tape speed). The incoming clock signal is a square wave switching between the "1" and "0" limits where "1" is nominally equivalent to +5V and "0" is nominally equivalent to 0V. If we define the incoming clock signal by the symbol C_L then the inverted clock signal C_L' will be displaced in time by half a clock period.

Each record is composed of up to 20 words which will be designated by the symbols W0 to W19 where the first bit in each word is B0 (defined above). As will be shown in Sec. B2.4.5 relating to the Programmer the "word counter" is advanced at bit time B9. The period starting at the leading edge of B9 of one word and ending at the trailing edge of B8 in the following word will be given the designation W_0 to W_{19} where the identification numbers are subscripts. Thus word W3, for instance, comprises bit times B0 to B8 of W_2 and bit times B9 to B19 of W_3. The logic meaning to be associated with W_0 to W_{19} is the same as that defined above for B0 to B19. All logic circuits relating to word times will utilize the word counter outputs W_0 to W_{19}.

W0 is the synchronizing word, W1 is the word relating to the run identification, W2 and W3 are words providing the time information (i.e. time of day, day of the month and month of the year) and W4 to W19 are the words associated with the Analogue to Digital Converter.

The first 16 bits (B0 to B15) of each word (except W0) contain all the required information. Simultaneously odd lateral parity checkbits are generated to enable recording on another track (Fig. 13). Even longitudinal parity checkbits are required at the end of each word. If the total number of bits preceding the longitudinal parity checkbit is even (16 for instance) then it is not possible to provide even longitudinal parity checkbits on both the data and lateral parity channels and at the same time fulfil the odd lateral parity requirement. Since odd lateral parity is required to enable the generation of clock pulses on replay (using OR logic) the above behaviour would not be acceptable. By recording an extra "dummy" character at time B16 and then recording even longitudinal check characters on the data and parity tracks at time B17 the lateral parity condition is met. Fig. 21 illustrates how this condition is satisfied.

The operation of the serial output portion of the Output Format Generator may be studied with reference to Fig. 20. The various integrated circuits have been assigned the letter "Q" followed by an identification number. Further details on the integrated circuits and a manufacturer's type numbers for suitable devices are given in the Appendix.

The input registers (Fig. 20) are designated by the letters "A," "B," "C," and "D." Registers A, B, and C are contained in the Digital Clock (Refer to Sec. B2.4.3 and Fig. 18) and register D is contained in the Analogue to Digital Converter. Run number identification is provided by register A, time information is provided by registers B and C and the output of the ADC is taken to register D. At a time corresponding to B17 (equivalent to C16 of the bit counter to be discussed in Sec. B2.4.5) of the word W1 the contents of register A are transferred to the shift register made up of flip flops Q30A to Q37B. Similarly at time B17 of words W2 and W3 information is transferred from registers B and C to the shift register. At all other times (written logically as $[W1 + W2 + W3]'$) information is transferred from register D to the shift register. In Fig. 20 the logic circuits which provide input register selection make use of W_1, W_2, and W_3 (i.e. subscripted) which, as defined earlier, refers to "word counter" outputs. This is quite acceptable as W1 and W_1 are simultaneously true at the bit time of interest B17, and similarly for W_2 and W_3.

The digital data is entered into the shift register via the preset lines. A logical 0 on the preset line sets the Q output of the shift register flip flops to logical 1.

The output flip flops Q29A and Q29B (see Fig. 20) have their J and K inputs shorted and connected to the Q and $\bar{Q}$ outputs respectively of the final stage of the shift register. If the Q output of Q30A is at logical 1 then application of a clock pulse to Q29A will cause this flip flop to toggle. If the Q output of Q30A is at logical 0 then application of a clock pulse to Q29A will not change its output. However Q29B will toggle because its J and K inputs are at logical 1. Hence the odd lateral parity condition is fulfilled.

Each time the shift register receives a clock pulse the pattern in the register moves one place to the right. The J and K inputs of Q37B are connected to logical 0 and logical 1 respectively. In this way each stage of the shift register, starting from Q37B, is consecutively reset (Q output at logical 0). In order to shift the last information bit from Q37B to Q30A 15 clock pulses are required. If an additional clock pulse is applied Q30A will also be reset and the "dummy" bit described earlier is provided. Hence of the 20 clock pulses (provided by incoming clock C_L) per word only 16 are required for the shift register and the shift register clock must be inhibited for the remaining 4. Clock pulses are provided corresponding to B1 to B16 but are inhibited for B17, B18, B19 and B0. Clocking for the shift register is in phase with the C_L input. The inhibit signal E_1 for the shift register clock (Fig. 20) is discussed in Sec. B2.4.5.

To allow the shift register time to settle, clocking of the output flip flops is made to lag half of a bit duration behind the shift register clock. In other words the clock signal for the output flip flops is in phase with C_L'. For all words, except W0, the output flip flops require clock pulses for bits B0 to B16 (one additional clock pulse to the number required by the shift register). For bit times B17, B18 and B19, and for the duration of the synchronizing word W0, the clock for the output flip flops must be inhibited, which is required to provide the "blank" signal to be recorded at this time. The inhibit signal I_1 (Fig. 20) for the output flip flop clock will be discussed in Sec. B2.4.5.

The outputs from Q29A and Q29B which are of NRZI form provide the data and the lateral parity outputs respectively. At B17 the output flip flops receive a pulse on the preset lines which resets the Q outputs to logical 0 (if not already in that state). The character generated constitutes the longitudinal parity check character. Either Q29A or Q29B (but not both) will change state at this time (Fig. 21).

It is to be noted that the digital output from the ADC is entered into the shift register during W0 (the synchronizing word). The shift register also receives clock pulses during W0. However the outputs from Q29A and Q29B are held at logical 0 as no clock pulses are received by these flip flops at this time.

The operation of the "parallel output" section of the Output Format Generator may be studied with reference to Fig. 22. In this case the 16 bit input words are divided up into three 6 bit words (2 additional zeros added). The addition of odd lateral parity checkbits provides 7 bit words suitable for recording on a 7 track recorder. Flip flops Q40A to Q47B make up four 3-bit shift registers and two 2-bit shift registers. Information is entered into these flip flops in exactly the same manner as for the "serial output" of Fig. 20; the timing and the logic is the same.

The outputs of shift register flip flops Q40A to Q42B are taken to the odd parity generator and to the output flip flops Q48A to Q50B.

If there is an odd number of ones at the input to the parity generator then the output will be a zero and vice versa. Appropriate logic circuits for providing the odd parity output are drawn in Fig. 23.

For each word three clock pulses are required for the output flip flops and two clock pulses are required for the shift registers. Longitudinal check characters are not generated. It is convenient to divide each word up into four periods and provide clocks pulses at (say) B4, B9 and B14 for the output flip flops and at B9 and B14 for the shift registers. A blank will effectively be recorded at B19 and will constitute a word separator.

The operation of the output flip flops is similar to that described earlier for the "serial output." The Ch. 1 to Ch. 7 outputs indicated in Fig. 22 are of NRZI form.

Since there are only 4 bit positions per word for the "parallel output" and there are 20 bit positions per word for the "serial output" a 5 : 1 reduction in data rate is obtained. Moreover the data packing density for the parallel record system (detailed in Sec. B2.1) can be made

approximately 500 bpi whereas that for the serial recording has been made 333⅓ bpi. The net effect is that when parallel recording is employed the tape speed may be reduced to 1/7·5 (probably can be extended to ⅛) of the speed required for the equivalent serial recording. Hence if, for instance, a recording were required at 1000 words per second the tape would have to be run at 60 ips for the serial recording or 7½ ips (probably) for the parallel recording. If 3600 ft tape reels were used respective maximum recording times per reel of tape would be 12 minutes and 96 minutes. In certain recording applications the increased recording time may be a great advantage.

A desirable feature of the 7 channel parallel recording system is that it provides a recording very similar to those normally read on most digital tape machines. It is possible that the parallel recording under discussion may be read by a suitable commercial digital tape machine.

B2.4.5. Programmer

The block diagram of Fig. 14 shows the Programmer in relation to the other equipment constituting the Airborne Digital Data Acquisition System. The function of the Programmer is to:

(i) Provide clock inhibit signals, input register select signals, and a data transfer signal for use with the Output Format Generator.

(ii) Provide switching signals for each multiplexer channel, and also a group switching signal (required for every 5 multiplexer channels).

(iii) Provide a "command to convert" signal and range select signals (programmed range mode of operation only) for the Analogue to Digital Converter.

(iv) Provide thumbwheel switch selection of the number of channels multiplexed or the number of words per record.

The requirements of a suitable programmer are analysed in this section and appropriate circuits are described.

In order to provide the control signals mentioned above two counters are required. The first, referred to as the "BIT COUNTER" has the clock signal C_L as its input and is basically a divide-by-20 circuit. The second, referred to as the "WORD COUNTER", has as its input an output from the bit counter (of frequency $C_L/20$). Division by any number up to a maximum of 20 is possible with this counter. Setting of two decade thumbwheel switches enables this number to be selected.

The bit counter can conveniently be made as a ripple type using a J-K flip flop as a divide-by-2 circuit in series with a decade counter (which is now readily available as a single package integrated circuit). The outputs from the decade counter are in 1-2-4-8 BCD code; the inverted outputs are not available. Let A_1, B_1, C_1, D_1 and E_1 be the outputs of each stage respectively. For details of the circuit configuration refer to Fig. 24.

In the following table the logical outputs of the bit counter are given as a function of count number. The numbers prefixed with the letter "C" are the decimal equivalent of the numbers registered in the counter. The numbers prefixed with the letter "B" refer to bit numbers where B0 is the first data bit and B15 is the last data bit. Corresponding "C" and 'B" numbers differ by unity. In the last column headed "Comments" the functions to be performed at the various bit times are indicated.

Bit Designation	Counter Designation	Logical Outputs					Comments
		E_1	D_1	C_1	B_1	A_1	
B1	C0	0	0	0	0	0	Second Data Bit—Serial Output
B2	C1	0	0	0	0	1	
B3	C2	0	0	0	1	0	
B4	C3	0	0	0	1	1	Clock for Parallel Output
B5	C4	0	0	1	0	0	
B6	C5	0	0	1	0	1	
B7	C6	0	0	1	1	0	
B8	C7	0	0	1	1	1	
B9	C8	0	1	0	0	0	Word Counter Advance. Clock for Parallel Output
B10	C9	0	1	0	0	1	
B11	C10	0	1	0	1	0	
B12	C11	0	1	0	1	1	
B13	C12	0	1	1	0	0	
B14	C13	0	1	1	0	1	Clock for Parallel Output
B15	C14	0	1	1	1	0	Last Data Bit—Serial Output
B16	C15	0	1	1	1	1	Dummy Bit—Serial Output
B17	C16	1	0	0	0	0	Data Entry into Shift Registers
							Longitudinal Parity—Serial Output
B18	C17	1	0	0	0	1	ADC Conversion Start
B19	C18	1	0	0	1	0	
B0	C19	1	0	0	1	1	First Data Bit—Serial Output
B1	C0	0	0	0	0	0	Second Data Bit—Serial Output

* Inhibit for output flip flop clock (Serial output only).
† Inhibit for shift register clock (Serial output only).

The output E_1 from the decade counter may be used to provide the inhibit signal for the shift register used for the serial output. By passing E_1 and C_L' through a NOR gate an output $C_L E_1'$ constituting the required shift register clock signal (Fig. 20) is obtained.

As discussed in Sec. B2.4.4 relating to the "serial output," the clock for the output flip flops is to be inhibited during bit times B17, B18 and B19 (or C16, C17 and C18) and also for the duration of the synchronizing word W0. The output D_1 from the bit counter is the input to the word counter and hence switching of the word counter occurs at bit time B9 (or C8).

The synchronizing word period W0 will overlap from W_0 into W_1 (for definition of W0, W_0 etc. refer to Sec. B2.4.4). In logic terms we may write

$$W0 = W_{19}(D_1 + E_1)' + W_0(D_1 + E_1)$$

From the previous table it can be seen that the combined C16, C17 and C18 times can be written logically as

$$C16 + C17 + C18 = A_1B_1'E_1$$

The complete inhibit signal for the output flip flops (serial output) is given by

$$I_1 = A_1B_1'E_1 + W0$$

$$= A_1B_1'E_1 + W_0(D_1 + E_1) + W_{19}(D_1 + E_1)'$$

Note that if the word counter is set to divide by less than 20 then W_{19} will be replaced by the last word output generated before the counter is reset.

Fig. 20 indicates that the inhibit signal I_1 together with the clock signal C_L are passed through a NOR gate. The output of the NOR gate, $C_L'I_1'$, provides the desired clock signal in phase with C_L' and inhibited when I_1 is true. The logic required to provide the I_1 signal is drawn in Fig. 25.

Setting of the shift register (serial output) and generation of the longitudinal parity checkbit is required at C16. Logically C16 may be written as

$$C16 = (A_1 + B_1)'E_1$$

The logic required to generate C16 is indicated in Fig. 25.

The control signals required by the "parallel output" section of the Output Format Genarator are:

(i) Clock signals in phase with C_L at bit times C8 and C13 for the shift registers.

(ii) Clock signals in phase with C_L' at bit times C3, C8 and C13 (except for the duration of the synchronizing word W0) for the output flip flops.

Logically we may write:

$$C8 + C13 = B_1'D_1(A_1C_1 + A_1'C_1')$$

Fig. 25 illustrates how (C8 + C13)' may be generated. By passing (C8 + C13)' together with C_L' through a NOR gate (Fig. 22) the required shift register clock signal $(C8 + C13)C_L$ may be generated.

For the output flip flops the required clock signal is given by $(C3 + C8 + C13)(W0)'C_L'$ where W0 is as determined previously in relation to the I_1 signal. The logic required to derive the above clock signal is indicated in Figs. 25 and 22.

At bit time C17 a "conversion start" signal initiates the conversion in the ADC the control circuits of which are indicated in Fig. 26. In the programmed range mode of operation the appropriate range is selected by a 12 position thumbwheel switch ("0" position not used) having a 1-2-4-8 BCD output.

Logically we can write:

$$C17 = A_1B_1'E_1$$

The logic circuits required to generate C17 are indicated in Fig. 25.

Decoded outputs are required from the word counter to provide gate signals associated with each word for switching of the Multiplexer and for control of the Output Format Generator. In addition the Multiplexer requires a group switching signal taking up 5 word times. The word counter has been drawn in Fig. 27. Basically the counter is a ripple type consisting of a decade divider (comprising A_2, B_2, C_2, and D_2) followed by a simple divide-by-2 circuit (E_2). Presetting of the maximum count to any number below 20 is possible using the thumbwheel switches (Fig. 27) which accept as inputs the BCD outputs from the counter and provide an output which is normally "0" but which switches to "1" when the decimal equivalent of the incoming data is the same as the number set on the thumbwheel switch.

Clock pulses for the word counter are derived from the D_1 output of the bit counter. The D_1 signal is first passed to the monostable Q66 which provides a narrow clock pulse for the counter. When coincidence between the digital input data and the number set on the thumbwheel switch occurs, the output of the NOR gate connected to the outputs of each thumbwheel switch reverts to the "0" state. The clock pulse is, under these conditions, inhibited from passing to the first flip flop Q56B and a logical 0 appears on the counter preset line for the duration of the monostable multivibrator output pulse. Hence the counter is preset and counting starts from zero again.

In the following table the logical outputs A_2, B_2, C_2, D_2 and E_2 are tabulated as a function of the word count.

WORD COUNTER TABLE

Count Number	Counter Output Designation	Logical Outputs				
		E_2	D_2	C_2	B_2	A_2
0	W0	0	0	0	0	0
1	W1	0	0	0	0	1
2	W2	0	0	0	1	0
3	W3	0	0	0	1	1
4	W4	0	0	1	0	0
5	W5	0	0	1	0	1
6	W6	0	0	1	1	0
7	W7	0	0	1	1	1
8	W8	0	1	0	0	0
9	W9	0	1	0	0	1
10	W10	1	0	0	0	0
11	W11	1	0	0	0	1
12	W12	1	0	0	1	0
13	W13	1	0	0	1	1
14	W14	1	0	1	0	0
15	W15	1	0	1	0	1
16	W16	1	0	1	1	0
17	W17	1	0	1	1	1
18	W18	1	1	0	0	0
19	W19	1	1	0	0	1
0	W0	0	0	0	0	0

Decoding of the word counter outputs to obtain the individual gate signals W_0 to W_{19} can be readily accomplished using a BCD to decimal decoder associated with outputs A_2, B_2, C_2 and D_2, and NOR gates associated with the decimal output from the decoder and the E_2 and E_2' outputs. In Fig. 28 the decoding arrangement has been drawn.

The multiplexer accepts the channel gating signals W_0 to W_{19} as illustrated in Fig. 29. As indicated in this figure the switching units are made up into batches of 5 which are required if a multiplexer of the type offered by Dynamics Systems Electronics Corporation and described in Sec. B2.4.1 is used. The outputs of each batch of switches is passed through another switch, designated MUX21 which is gated by inputs P, Q, R and S where

$$P = W_5 + W_6 + W_7 + W_8 + W_9$$

$$Q = W_{10} + W_{11} + W_{12} + W_{13} + W_{14}$$

$$R = W_{15} + W_{16} + W_{17} + W_{18} + W_{19}$$

$$S = W_0 + W_1 + W_2 + W_3 + W_4$$

It is to be noted that the batch of switches designated MUX14 (Fig. 29) has been drawn with W_0, W_1, W_2 and W_3 as inputs (dotted). Normally these signals would be used as indicated in Sec. B2.4.4 but may equally be used to switch analogue data signals if desired.

From the word counter table we may write:

$$P = E_2'Y_2$$

$$Q = E_2Y_1$$

$$R = E_2Y_2$$

$$S = E_2'Y_1$$

$$\text{where } Y_1 = D_2'(A_2'B_2'C_2' + A_2B_2'C_2' + A_2'B_2C_2' + A_2B_2C_2' + A_2'B_2'C_2)$$
$$= D_2'(B_2'C_2' + B_2C_2' + A_2'B_2'C_2)$$
$$= D_2'(C_2' + A_2'B_2'C_2)$$
$$= D_2'(C_2' + C_2'A_2'B_2' + A_2'B_2'C_2)$$
$$= D_2'(A_2'B_2' + C_2')$$
$$\text{and } Y_2 = C_2D_2'(A_2B_2' + A_2'B_2 + A_2B_2) + B_2'C_2'D_2(A_2 + A_2')$$
$$= C_2D_2'(A_2 + A_2'B_2) + B_2'C_2'D_2$$
$$= (A_2 + B_2)C_2D_2' + B_2'C_2'D_2$$

The logic circuits required to produce the group switching signals P, Q, R and S have been drawn in Fig. 30. It is to be noted that group switching signals could have been readily provided if the word counter had utilized a divide-by-5 and a divide-by-4 circuit in cascade. However, such a counter could not readily be used in conjunction with decimal thumbwheel switches for setting the number of channels to be multiplexed (or the total number of words). Moreover a BCD to decimal decoder (a commercially available integrated circuit) could not be used with such a counter.

B2.4.6. Record Head Amplifiers

Record head amplifiers, driven by the NRZI outputs of the Output Format Generator, are required to provide suitable current drive for the record head. For the system under development at these laboratories it is essential that the amplifiers plug directly into an Ampex Model AR200 Electronics Unit in the same way as the Direct, FM and PDM record cards.

Record amplifiers and a digital record head are available from Ampex Corporation for the seven channel parallel digital recording system. However, for serial digital recording using the existing analogue heads, no record amplifiers are available from Ampex Corporation and so the development of suitable amplifiers has been necessary. Two amplifiers are required, one for the data track and one for the lateral parity track.

NRZI recording requires that the tape be saturated consecutively in one direction then the other. Frequently digital recorders employ record head windings which are centre tapped. By connecting the centre tap to a supply rail and by switching current from one half winding to the other half winding an appropriate flux reversal is achieved. The appropriate driving signal can be readily provided if each half winding is connected to alternate outputs of a flip flop. In contrast the analogue record heads for the Ampex Model AR200 utilize single windings and hence current reversal must be provided. Since saturation flux may have to be maintained in one direction for a considerable period DC coupling to the head winding is essential.

An indication of the head current requirement may be obtained from measurements relative to the FM recording technique for which the tape is alternately saturated in each direction. Measurements made on the FM record cards indicated a head current requirement ranging from 40 mA (peak to peak) to 60 mA (peak to peak) for the complete range of centre frequency plug-ins and the complete range of FM record cards. Hence it has been decided to provide ± 30 mA for the NRZI digital recording. The record head impedance is quite low, varying from approximately 1·2 ohm at 10 Hz to about 80 ohm at 200 KHz.

Supplies of +22V and −20V are available at the record card sockets of the Model AR200. Of these the +22V supply has the better regulation and also has a much larger reserve of available power than the −20V supply. For this reason it has been decided that the digital record amplifiers operate solely from the +22V supply. When a single supply is used, it is necessary to establish a centre tap which can act as a source or sink for current.

An amplifier (Fig. 31) has been developed which will accept the single ended input signal to be provided by the Output Format Generator (Serial Output—see Fig. 20). Alternate switching of the complementary output transistors occurs as the input changes in level. When the upper transistor in the output stage switches "on," current flows from the +22V supply through the record head and into the +11V centre tap. When the lower transistor switches "on," current flows out of the +11V centre tap back to the common terminal.

All record amplifiers used in conjunction with the Model AR200 incorporate a 10-ohm resistor which is connected in series with the record head when the amplifier card is plugged into

the Electronics Unit. In every instance (except for the amplifier at present under discussion) one end of the 10-ohm resistor is returned to common. The voltage across the 10-ohm resistor is in phase with the record head current and enables the latter to be examined using with the Test Set which is used for checking the Model AR200 prior to recording data. Accidental shorting of the record head to common is quite possible while the Test Set is being used. For the digital record amplifier in question shorting of the record head to common would mean effectively shorting the +11V centre tap to common. It is therefore essential that the +11V supply be able to accommodate a sustained short circuit without producing damage to either the regulator or the external circuit (e.g. record head).

In Fig. 32 the circuit of the centre tap power supply has been drawn. The circuit represents a true centre tap as the regulator circuit utilizes the incoming +22V supply as a reference. If the potentiometer is set to provide an output equal to half the input voltage then the condition will also be satisfied if the input voltage happens to shift. The basic supply is loaded with a 150-ohm resistor to ensure that the regulating transistors are conducting even when current is flowing into the centre tap supply. Overload circuits are incorporated which cause both output voltage and output current to fall if one attemts to increase the output current beyond about 70 mA (sufficient for two amplifiers). When the output is shorted the current through the short circuit is 6·3 mA.

The centre tap regulator has been designed to drive two amplifiers required for the data and parity tracks respectively.

B3. MONITOR FACILITY

The Ampex Model AR200 Recorder used by these laboratories for airborne data acquisition is basically manufactured as a record only device but it has been designed (by the manufacturers) to take a "Monitor" head assembly in addition to the normal record head assembly. Cabling from the monitor head socket to an external socket has been incorporated in the recorder. The monitor heads are of normal IRIG specification and are, in effect, playback heads.

At present records made using the Model AR200 Recorder cannot be checked until the magnetic tapes have been returned to the laboratories. In many airborne trials it is essential that virtually 100% reliability be obtained in the recording process as repetition of tests is frequently not possible or, if possible, is very expensive. The ability to check that data has been properly recorded in these circumstances represents quite an advantage.

For reasons detailed above it has been decided to extend the recording facilities to enable a "quick look" of recorded data to be obtained in the field. To realize the above, a "Monitor Facility" is at present under development.

It has been found impractical to install pre-amplifiers for the low level reproduce signals in the Ampex Model AR200 Tape Transport Unit. Pre-amplifiers similar to those used at present in the Ampex Model FR1200 Recorder/Reproducer have been built at these laboratories and will be installed in the Monitor Unit at present under construction. The low level reproduce signals will be taken to the Monitor Unit via a cable made up of shielded and insulated two-wire units.

It is intended that Ampex Model FR1200 reproduce plug-ins be used to provide readable outputs from the monitor unit. The outputs of the pre-amplifiers may be connected directly to the inputs of the reproduce plug-ins.

Both the reproduce pre-amplifiers and the Model FR1200 Reproduce Plug-ins require regulated supplies of +12V and −12V. To avoid the need for a separate battery or power unit for the monitor facility it is desirable that power be derived from the existing system. Regulated supplies of +12V and −12V are not available from the recorder, but a reserve of power can be taken from the +22V and the −20V supplies available in the Model AR200 to regulators adjusted to give outputs of +12V and −12V. A power outlet socket is available on the Model AR200 Electronics Unit which is designed to couple to a second unit when a 14-channel system is used. Power for the Monitor Unit can be readily derived from this outlet.

It is not considered necessary to be able to view the outputs of all seven channels simultaneously; viewing of one channel at a time is usually adequate. The Monitor Unit has been designed to take a Direct, an FM and a PDM Reproduce Card. Selection of the appropriate reproduce card is made via a switch. Channel selection is made via a switch which selects the

appropriate pre-amplifier output. In addition the Monitor Unit will take a fourth reproduce card which is normally used for monitoring speech commentaries. A battery operated amplifier and speaker combination has been designed to enable speech commentaries to be listened to. Usually the outputs will be measured with a suitable voltmeter or viewed on a Cathode Ray Oscilloscope.

In addition to providing a "quick look" capability the Monitor Unit can also be used for some very limited data reduction. Because of the lack of rewind facilities it is very awkward to use the Model AR200 in this mode.

B4. PROPOSAL FOR DATA REDUCTION

Normally data reduction is performed at a suitable ground station and as such the data reduction equipment does not have to meet the stringent environmental requirements laid down for the airborne equipment. Since the data reduction requirements cover a vast field they have been made the subject of another paper[32] to be published later. A brief outline, only, of the data reduction requirements will be given here.

Since in all cases (except that of seven-channel digital recording) recording is made using analogue heads it is essential that an analogue tape reproduce machine is available. It is desirable that the reproducer also accept tape loops which are frequently required for detailed analysis of data recorded using analogue techniques. It is essential that a servo speed control of the instantaneous "variety" (Sec. B1.2) be incorporated to realize improved signal to noise ratios for the FM system of recording. Analogue reproduce machines having these characteristics are available commercially.

As indicated in Sec. B1.1 it is intended that speech and a reference frequency be recorded on a single direct record channel. Special replay equipment (Sec. B1.1) has been developed for separating the speech and the reference frequency.

Some consideration is being given to the use of "flutter compensation" techniques on replay to further improve the signal to noise ratio for the FM system (Sec. B1.2).

Information relating to the frequency and the amplitude of the signal components is often required for data recorded using FM techniques. The type of equipment required for the analysis depends on the nature of the data as indicated below.

For periodic data (amplitude and frequency of components not changing with time) or for data which varies slowly with time a wave analyser with motorized or electronic frequency sweep is suitable. Usually such equipment effectively sweeps a narrow band pass filter characteristic through the frequency range of interest and provides simultaneous outputs corresponding to frequency and amplitude of signal component at that frequency.

For random data or for data containing discrete frequency components the amplitude of which changes fairly rapidly with time the wave analyser gives unreliable answers. Measurements of this type are better performed in terms of the "Power Spectral Density" (the long term distribution of the power in the wave plotted in the frequency domain). Equipment is available commercially for producing power spectral density plots using analogue techniques. Digital computer techniques may also be used. Pavia[33] discusses a suitable program for use with a Control Data Corporation Model 160-A digital computer.

For the PDM system reconstruction of the PDM record waveform is possible using a suitable analogue reproduce machine. Some possible decoding systems for PDM data have been discussed in Sec. B1.3.

The reduction of data recorded in digital form is best accomplished with the aid of a digital computer. In the case of the serial digital recording the data will first be read using an analogue tape machine (the data as recorded is not in computer compatible format and therefore cannot be read directly into a computer via a digital tape machine). The serial data as read from the analogue reproducer using suitable read amplifiers must firstly be arranged in parallel form. Since each word contains 16 information bits a 16 bit storage register should enable a word by word conversion to be implemented. Many of the digital computers available will, on command, read in a 16 bit word. A suitable serial to parallel converter incorporating parity checking circuits and providing appropriate synchronizing signals is required.

For the seven-channel parallel digital recording system, replay using a seven-channel digital in-line head would be necessary. In other respects the data reduction requirements are similar

to those for the serial recording, but the information would still require rearrangement into 16-bit parallel words for reading into a digital computer. There is a possibility that recordings could be read directly by a seven-channel digital machine, but this aspect would require investigation.

In some circumstances reading of time information, independently of the digital computer, may be required as for example if a real time scale were required for an analogue recording (FM recording for instance) to be reduced using analogue equipment. For such an application a Time Reader with an output suitable for recording on a chart recorder would be desirable. The Time Reader would enable accurate time correlation of data recorded by analogue means with data recorded by digital means.

Another advantage of a Time Reader is that it would enable any point of interest on the recording to be accurately located. For this purpose a digital output from the Reader in the form of an in-line display giving time in hours, minutes and seconds would be highly desirable. A little further development would enable the tape replay machine to be stopped when a preselected time had been reached.

Since the time information would occupy only 2 words per record of the digital recording it would be the function of the Time Reader to synchronize to the appropriate words and ignore the remainder of the digital information.

Reduction of the digital data will be performed with the aid of suitable computer programmes. One of the problems associated with the incoming digital data is that the time of day information will be in BCD code and the transducer data (or data encoded by way of the Analogue to Digital Converter) will be in pure binary code. Some difficulty may arise if the computer is expected to handle both codes simultaneously. To overcome this problem it may be desirable to convert, say, the BCD time of day information into a pure binary code prior to reading the information into the computer. Code conversion of this type would involve fairly complex equipment.

With the basic system as proposed above there are various lines of possible extension. At times, for instance, it may be desirable to process data, recorded using analogue techniques, digitally which would be accomplished using an analogue to digital converter operating on line to the digital computer. It is possible that the airborne ADC described in Sec. B2.4.2 may be of use in this regard when it is not required for data acquisition purposes.

Storage of data in the form of a computer compatible magnetic tape may be very desirable. To enable such data storage a magnetic tape peripheral unit would be required.

Suitable peripheral equipment such as a printer providing digital readout and a plotter which is capable of providing an analogue plot of one quantity as a function of another, will be required in conjunction with the digital computer. In a typical data reduction job it may be necessary to plot Mach Number, say (which is a function of several parameters recorded using digital techniques) as a function of time (which is also recorded using digital techniques).

CONCLUSION

A novel system of recording data in airborne applications has been described. Both analogue and digital data will be recorded on a single analogue magnetic tape recorder. The following recording techniques will be adopted:

(i) Direct recording will be used only for flight crew commentaries and reference frequencies because of its small dynamic range and low accuracy.

(ii) Frequency modulation recording will be used extensively for vibration, pressure and similar measurements where fairly large bandwidths and about 2% accuracy is required.

Increased accuracy is possible if servo speed control of the replay machine is incorporated. Even further improvements may be possible using flutter compensation techniques.

(iii) The pulse duration modulation system will be used for recording many channels of fairly low frequency data to 1% accuracy. This system will be used in preference to the digital system only when the required information packing density on the tape is higher than that obtainable with the digital system.

(iv) The digital (or pulse code modulation) system has been adopted for high accuracy (up to 0·1%) recording of many channels of low frequency data.

Time of day information will be recorded in digital form with the other multiplexed data. Time correlation between analogue and digital recordings will therefore be possible.

An analogue tape reproduce machine is necessary as a first stage in the reduction of both analogue and digital data. Reduction of analogue records will be performed with suitable analogue equipment and the reduction of digital records will generally be performed by a digital computer.

Postal Address: Chief Superintendent,
Aeronautical Research Laboratories,
Box 4331, P.O.,
MELBOURNE, Victoria, 3001.

REFERENCES

1. D. F. Eldridge — The Mechanism of A.C. Biased Magnetic Recording. I.R.E. Transactions on Audio. September-October 1961.

2. B. B. Bauer — A New Model for Magnetic Recording. I.R.E. Transactions on Audio. September-October 1961.

3. P. J. Weber — The Tape Recorder as an Instrumentation Device. Ampex Corporation Copyright 1959.

4. E. D. Daniel, P. E. Axon, and W. T. Frost — A Survey of Factors Limiting the Perromance of Magnetic Recording Systems. Proc. I.E.E. March 1957.

5. M. B. Martin — The Mechanical Considerations of Magnetic Recording Heads. Journal Brit. I.R.E. November 1960.

6. J. N. Borwick — The Characteristics and Applications of Magnetic Recording Tape. Part 1. Electronic Components. November 1963.

7. E. Franck — Magnetic Tape Dropouts. Instruments and Control Systems. March 1959.

8. R. Noble — Assessment of the Reliability of Magnetic Tape for Data Processing. Journal Brit. I.R.E. October 1960.

9. M. Camras — Current Problems in Magnetic Recording. Proc. I.R.E. May 1962.

10. D. H. Howling — Noise in Magnetic Recording Tapes. Journal of the Acoustical Society of America. September 1956.

11. W. B. Snow — Characteristics of Tape Noise. Audio. February 1961.

12. A. H. Moris — A New Magnetic Tape with Greater Dynamic Range. Journal of the Audio Engineering Society. January 1964.

13. P. A. Godinez and J. F. Muench — Phase Equalization. Leach Corporation Engineering Bulletin No. 107.

14. R. A. Wainwright — Correcting Phase Distortions in Magnetic Tape Recorders. Rixon Engineering Bulletin No. 71. January 1961.

15. G. Work and D. Lewis — Comparison of Wideband FM and Carrier Erase Techniques for Recording Data from DC to 10 KC. Leach Corporation Publication.

16. Telemetry Working Group of the Inter-Range Instrumentation Group — Telemetry Standards. IRIG Document No. 106-60.

17. P. A. Godinez — FM Bandwidth Utilization. Leach Corporation Engineering Bulletin No. 111.

18. P. A. Godinez — Flutter Compensation. Leach Corporation Engineering Bulletin No. 110.

19. G. W. Disbrey — Speed and Timing Errors in Tape Instrumentation. Instrument Practice. September 1964.

20. C. B. Pear — Flutter in Magnetic Recording of Data. I.R.E. Transactions on Audio. September-October 1961.

21. P. A. Godinez — Bandwidth and S/N in FM Systems. Leach Corporation Engineering Bulletin No. 112.

22. P. A. Godinez — Extended Bandwidth FM System. Leach Corporation Engineering Bulletin No. 114.

23. P. E. Axon — Instrumentation Magnetic Recording. Journal Brit. I.R.E. October 1960.

24. J. N. Borwick — The Characteristics and Applications of Magnetic Recording Tape. Part 2. Electronic Components. January 1964.

25. D. W. Halfhill — Recording Techniques. Instruments and Control Systems. March 1959.

26. P. A. Godinez — PCM Recording Techniques. Leach Corporation Engineering Bulletin No. 106.

27. — Pulse Code Modulation Applied to Data Storage and Transmission. Leach Corporation Publication. February 1964.

28. M. D. Card — System of Recording Speech and a Reference Frequency on a Single Track of an Airborne Tape Recorder. To be published at A.R.L.

29. S. W. Athey — Magnetic Tape Recording. NASA SP-5038. January 1966.

30. N. Steer — Project Ikara—Ship's Digital Encoding System (S.D.E.S.). Description, Operation and Maintenance Instructions Manual WRE 255.

31. Digital Equipment Corporation — Analogue—Digital Conversion Handbook E-5100. Copyright 1964.

32. K. F. Fraser — Data Reduction Requirements Relating to an Airborne Data Logger. To be published at A.R.L.

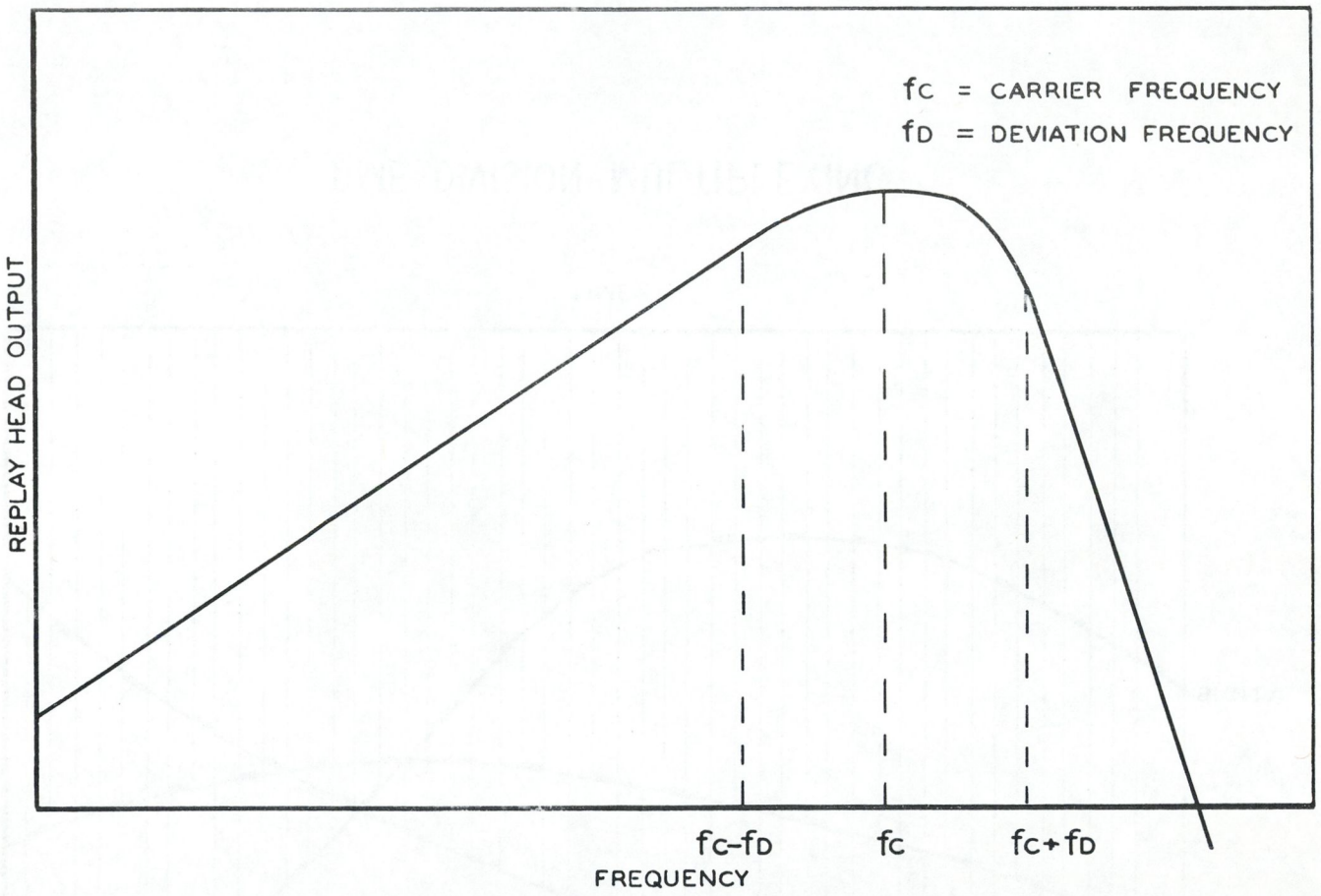
33. R. V. Pavia — A Computer Program for obtaining Power Spectral Density Plots from Voltage Analogue Signals. A.R.L. Tech. Memo/Mech. Eng. 311. August 1968.

APPENDIX

A list of integrated circuits referred to in Figs. 20, 22, 23, 24, 25, 27, 28 and 30 is given below. Each integrated circuit is marked with the letter "Q" followed by an identification number. In all cases the manufacturer's identification code refers to a device manufactured by Texas Instruments. It is appreciated that equivalent integrated circuits are in some instances available from other manufacturers. No attempt has been made to list code numbers of devices supplied by other manufacturers.

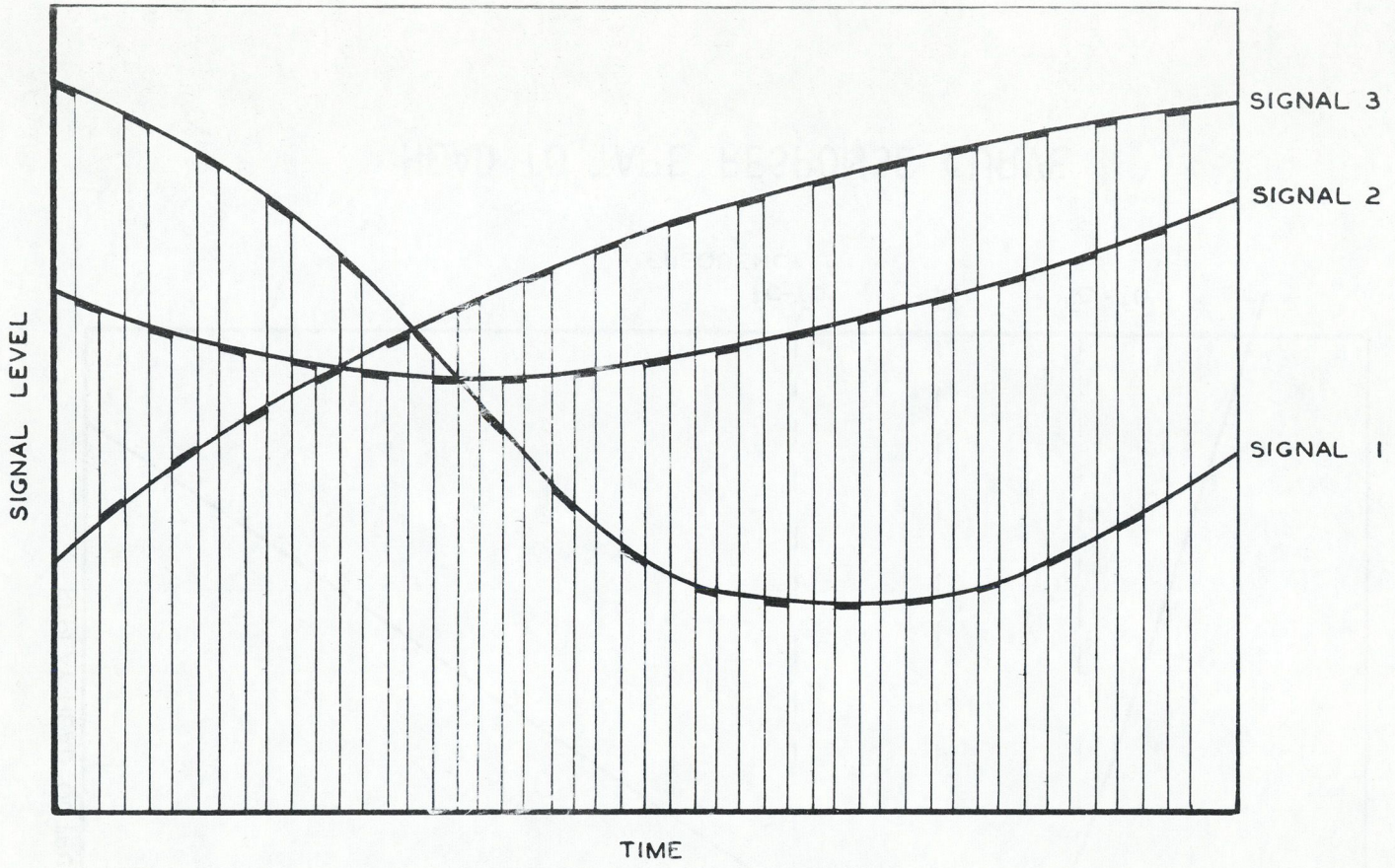
Legend	Manufacturer's Code	Logic Classification	Description
Q1	SN5400	TTL	Quadruple 2—Input Positive Nand Gate
Q2	SN5400		
Q3	SN5400		
Q4	SN5400		
Q5	SN5400		
Q6	SN5400		
Q7	SN5400		
Q8	SN5400		
Q9	SN5400		
Q10	SN5400		
Q11	SN5400		
Q12	SN5400		
Q13	SN5400		
Q14	SN5400		
Q15	SN5400		
Q16	SN5400		
Q17	SN5420	TTL	Dual 4—Input Positive Nand Gate
Q18	SN5420		
Q19	SN5420		
Q20	SN5420		
Q21	SN5420		
Q22	SN5420		
Q23	SN5420		
Q24	SN5420		
Q25	SN5400	TTL	Quadruple 2—Input Positive Nand Gate
Q26	SN5400		
Q27	SN5400		
Q28	SN5400		
Q29	SN5473	TTL	Dual J-K Master-Slave Flip-Flop
Q30	SN5473		
Q31	SN5473		
Q32	SN5473		
Q33	SN5473		
Q34	SN5473		
Q35	SN5473		
Q36	SN5473		

Legend	Manufacturer's Code	Logic Classification	Description
Q37	SN5473		
Q38	SN5402	TTL	Quadruple 2—Input Positive Nor Gate
Q39	SN5400	TTL	Quadruple 2—Input Positive Nand Gate
Q40	SN5473	TTL	Dual J-K Master-Slave Flip-Flop
Q41	SN5473		
Q42	SN5473		
Q43	SN5473		
Q44	SN5473		
Q45	SN5473		
Q46	SN5473		
Q47	SN5473		
Q48	SN5473		
Q49	SN5473		
Q50	SN5473		
Q51	SN5473		
Q52	SN5451	TTL	Dual 2 Wide 2—Input And-Or-Invert Gate
Q53	SN5451		
Q54	SN5451		
Q55	SN5400	TTL	Quadruple 2—Input Positive Nand Gate
Q56	SN5473	TTL	Dual J-K Master-Slave Flip-Flop
Q57	SN5490	TTL	Decade Counter
Q58	SN5400	TTL	Quadruple 2—Input Positive Nand Gate
Q59	SN5400		
Q60	SN5400		
Q61	SN5400		
Q62	SN5402	TTL	Quadruple 2—Input Positive Nor Gate
Q63	SN5402		
Q64	SN5473	TTL	Dual J-K Master-Slave Flip-Flop
Q65	SN5473		
Q66	SN5380	DTL	One-Shot Monostable Multivibrator
Q67	SN5402	TTL	Quadruple 2-Input Positive Nor Gate
Q68	SN5400	TTL	Quadruple 2-Input Positive Nand Gate
Q69	SN5442	TTL	BCD to Decimal Decoder
Q70	SN5402	TTL	Quadruple 2-Input Positive Nor Gate
Q71	SN5402		
Q72	SN5402		
Q73	SN5402		
Q74	SN5402		
Q75	SN5400	TTL	Quadruple 2-Input Positive Nand Gate
Q76	SN5402	TTL	Quadruple 2-Input Positive Nor Gate
Q77	SN5402		



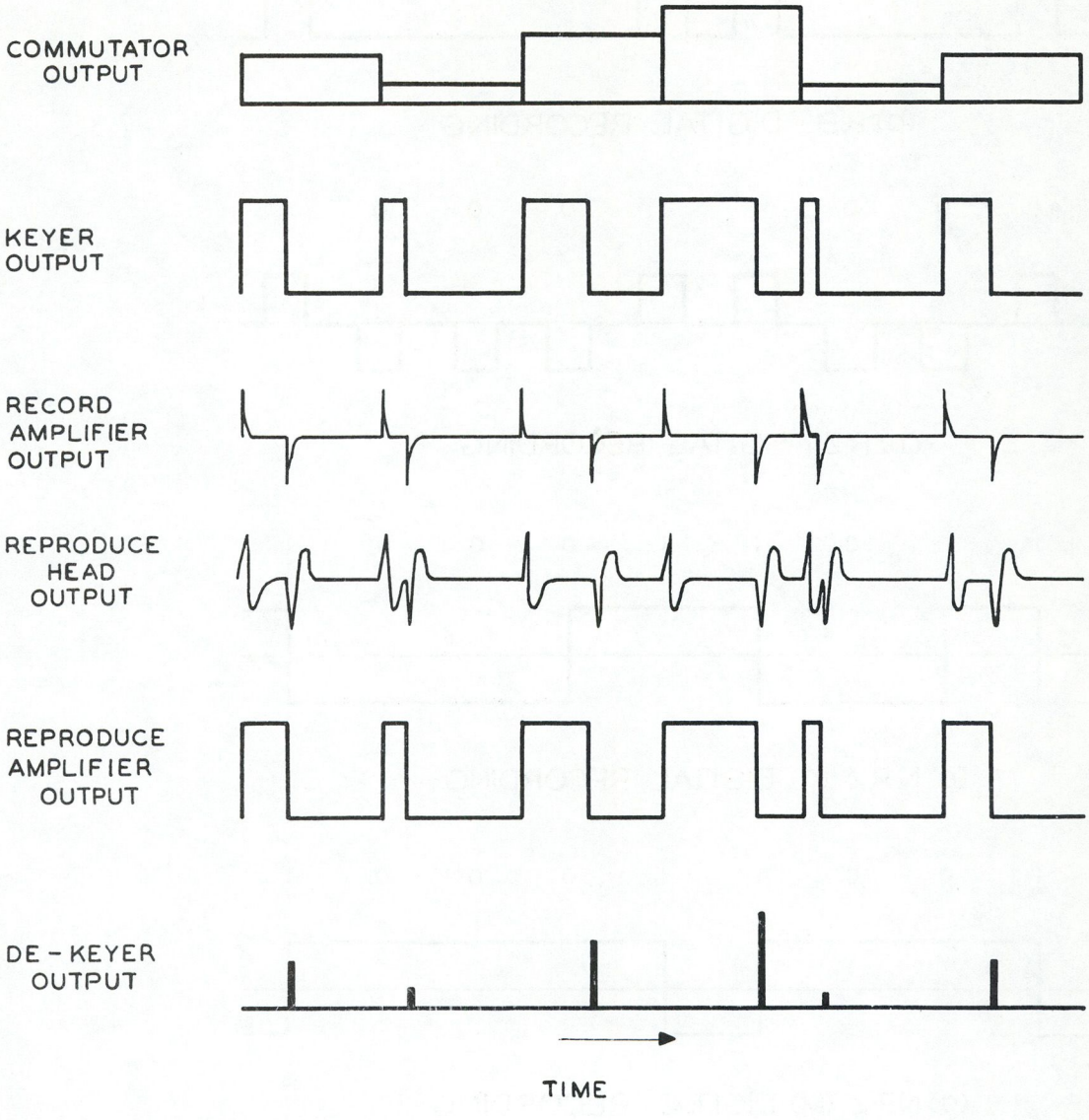
HEAD TO TAPE RESPONSE CURVE

REPORT M.E.126
FIG.1

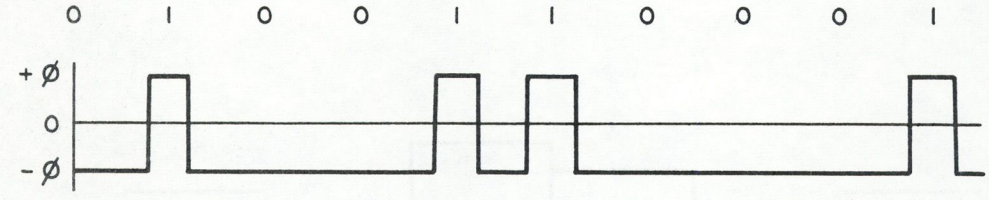


TIME DIVISION MULTIPLEXING

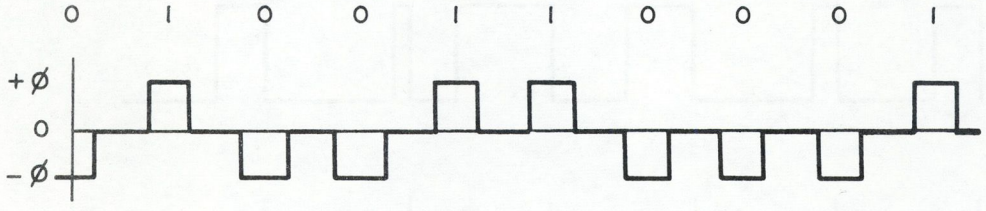
REPORT M.E.126
FIG.2



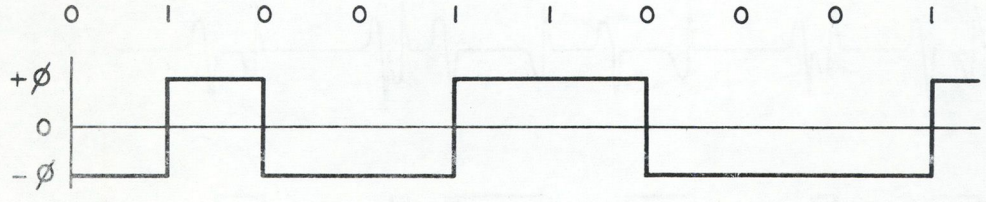
WAVEFORMS AT THE VARIOUS STAGES IN A PDM SYSTEM



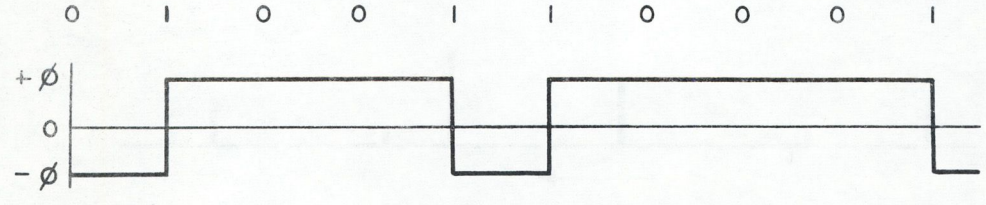
(a) RB DIGITAL RECORDING



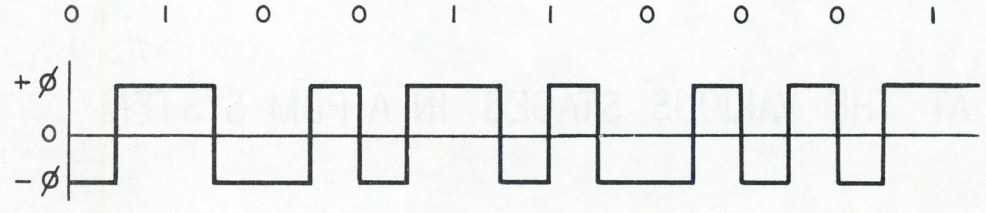
(b) RZ DIGITAL RECORDING



(c) NRZ (C) DIGITAL RECORDING

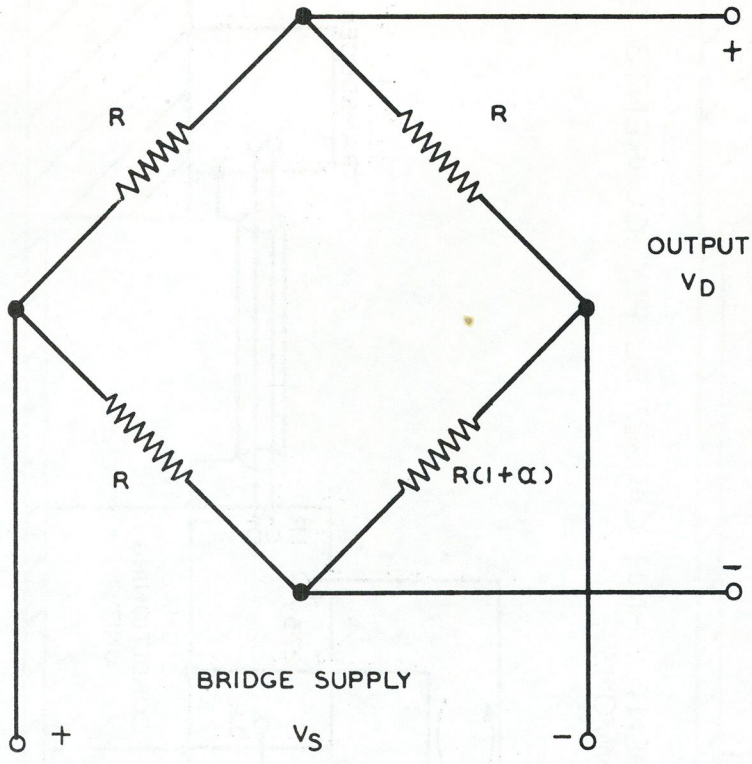


(d) NRZ (M) DIGITAL RECORDING

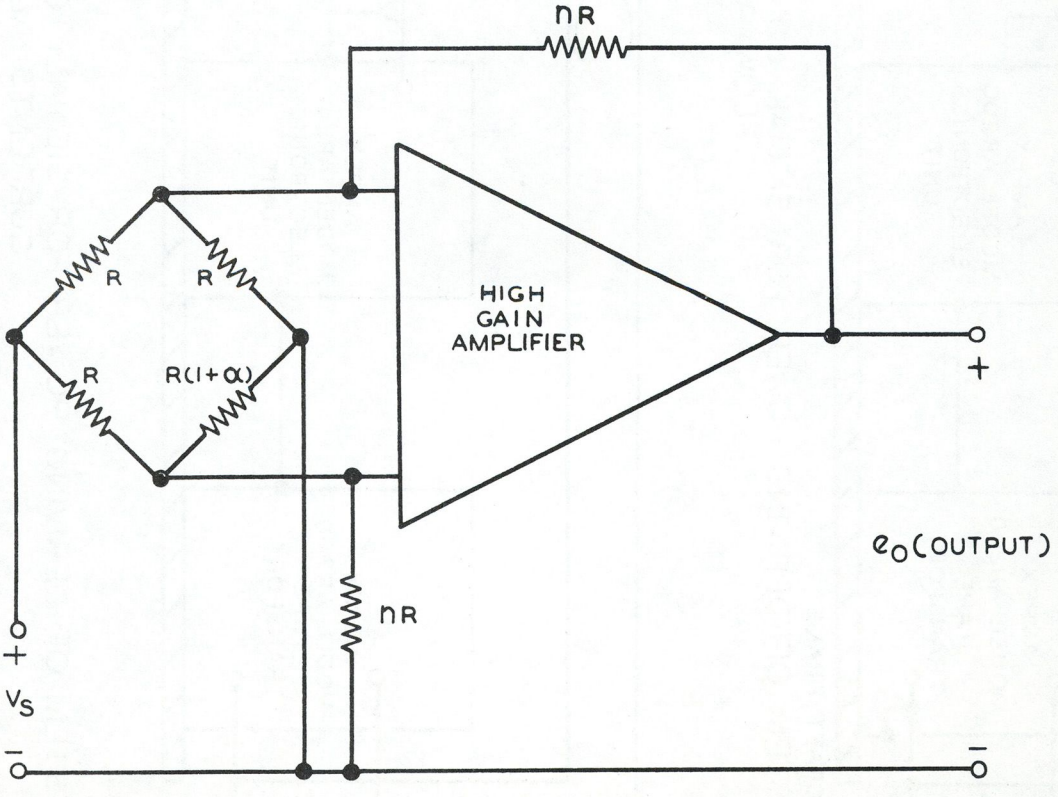


(e) MANCHESTER CODE DIGITAL RECORDING

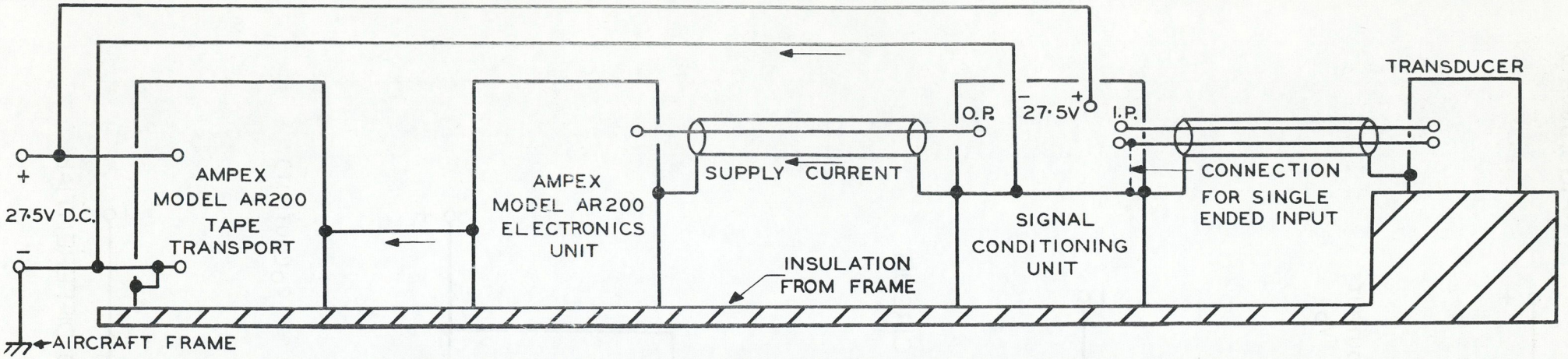
PCM RECORD SCHEMES



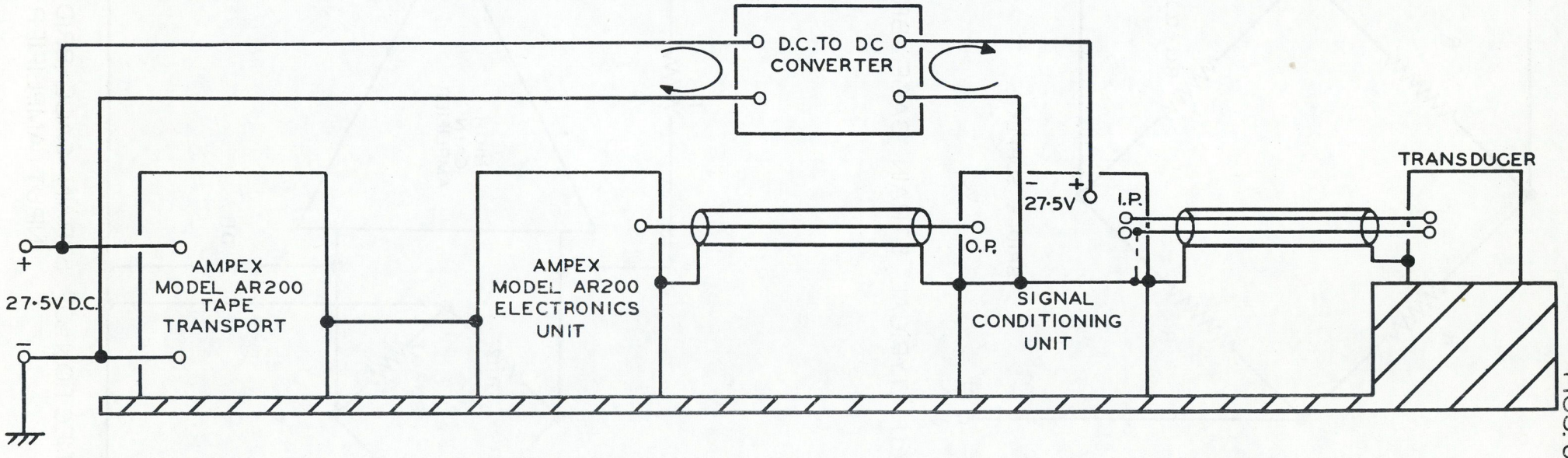
(a) TYPICAL STRAIN GAGE BRIDGE CIRCUIT



(b) CONNECTION OF STRAIN GAGE BRIDGE TO DIFFERENTIAL INPUT AMPLIFIER

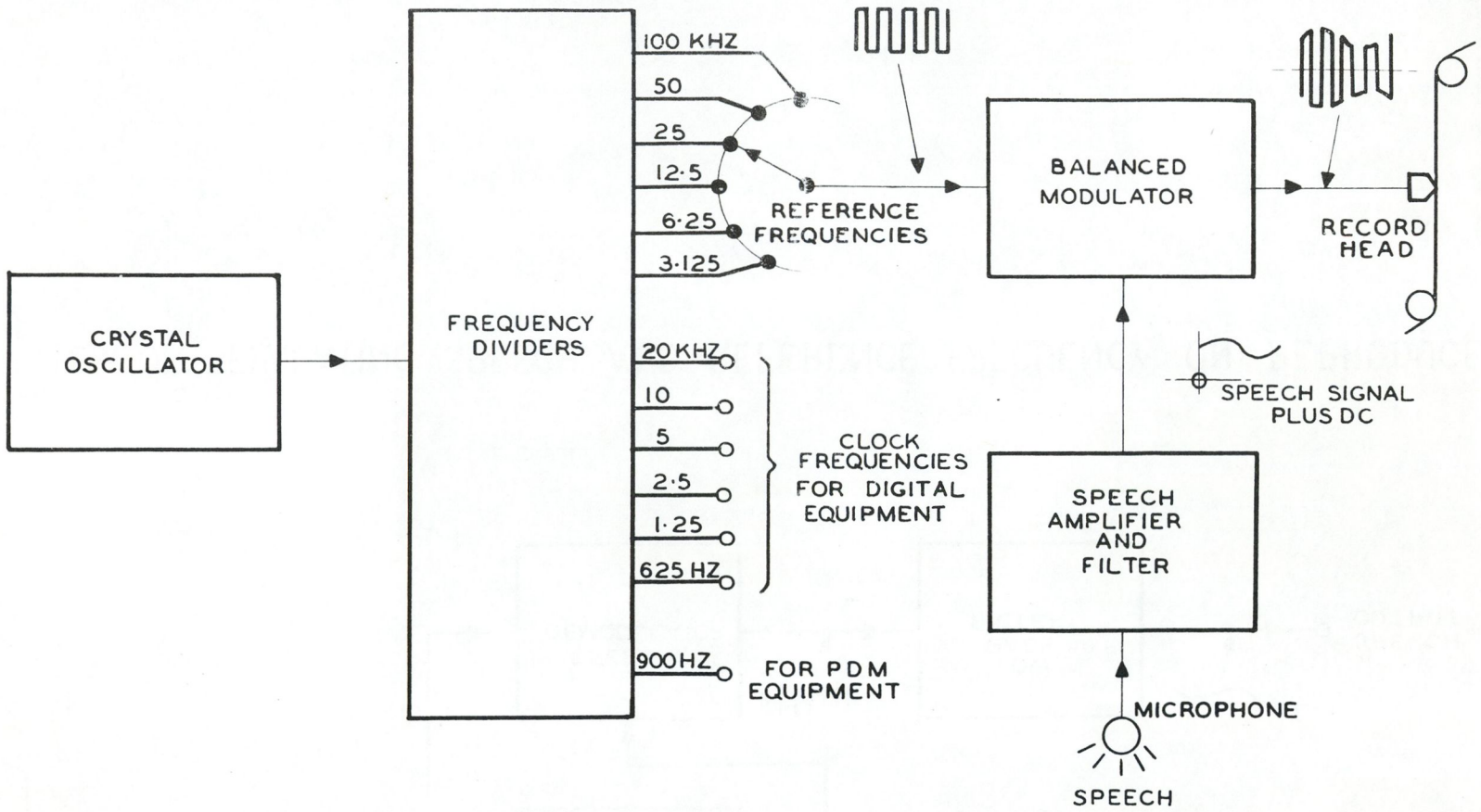


(a) SYSTEM OF DERIVING POWER FOR SIGNAL CONDITIONING EQUIPMENT WHICH CAUSES SUPPLY CURRENTS TO FLOW ALONG SIGNAL COMMONS



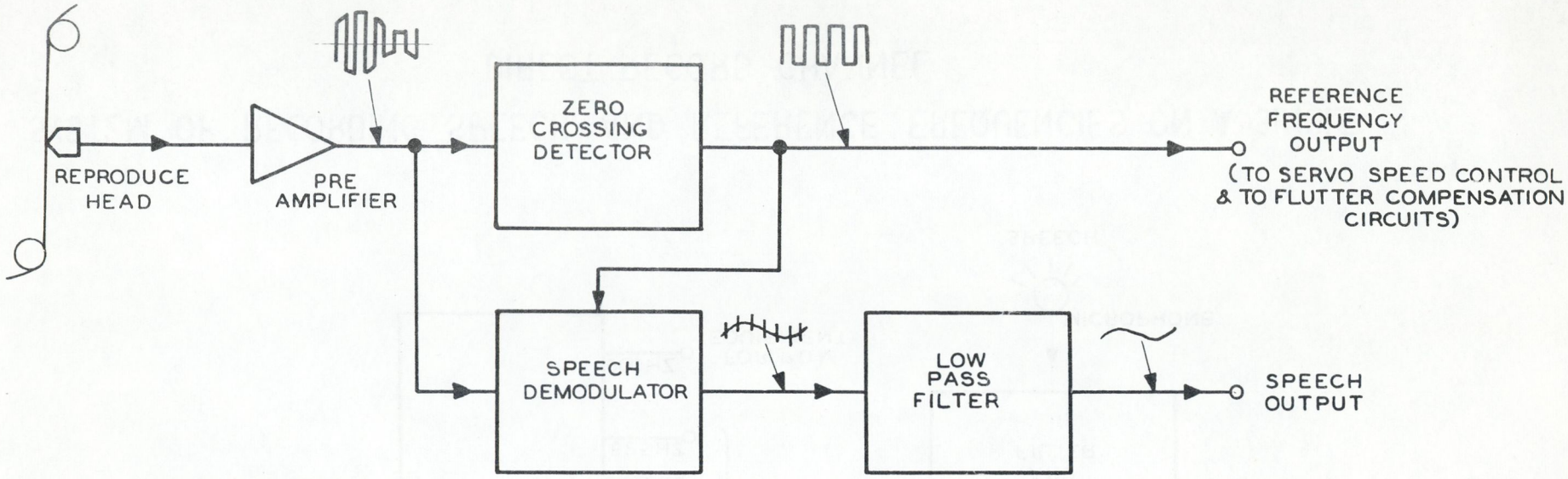
(b) SYSTEM OF DERIVING POWER FOR SIGNAL CONDITIONING EQUIPMENT WHICH PREVENTS FLOW OF SUPPLY CURRENTS ALONG THE SIGNAL COMMONS

REPORT M.E.126
FIGS. 6(a) & 6(b)



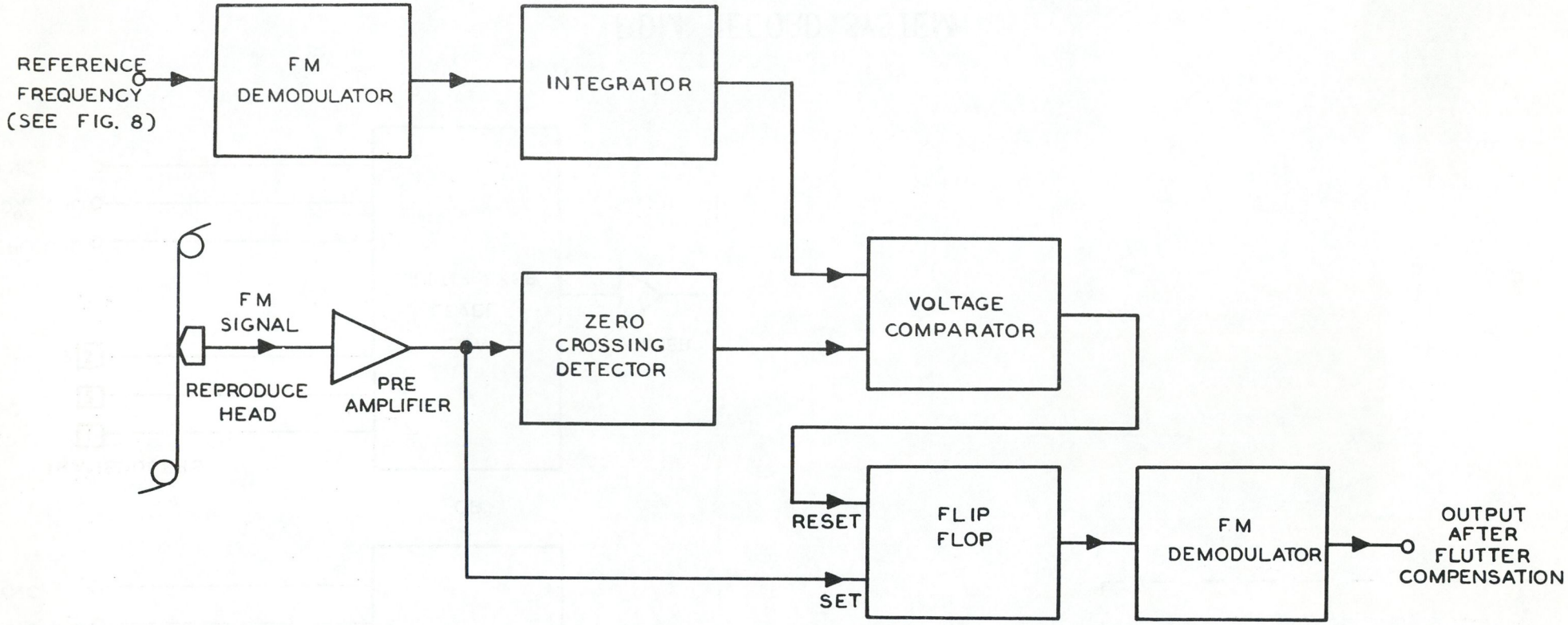
SYSTEM OF RECORDING SPEECH AND REFERENCE FREQUENCIES ON A SINGLE DIRECT RECORD CHANNEL

REPORT M.E. 126
FIG. 7



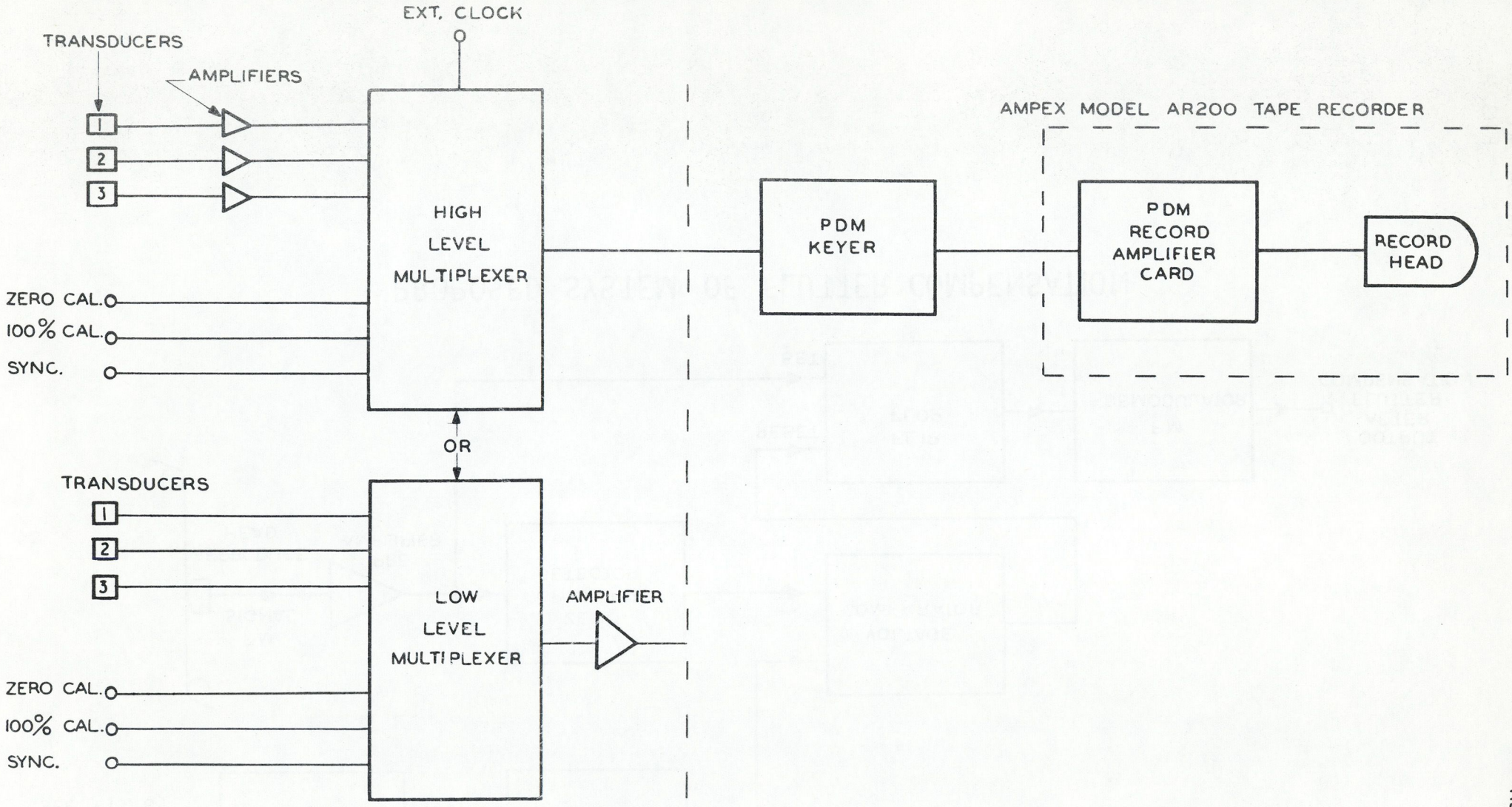
SYSTEM OF SEPARATING SPEECH AND REFERENCE FREQUENCY ON REPRODUCE

REPORT M.E.126
FIG.8



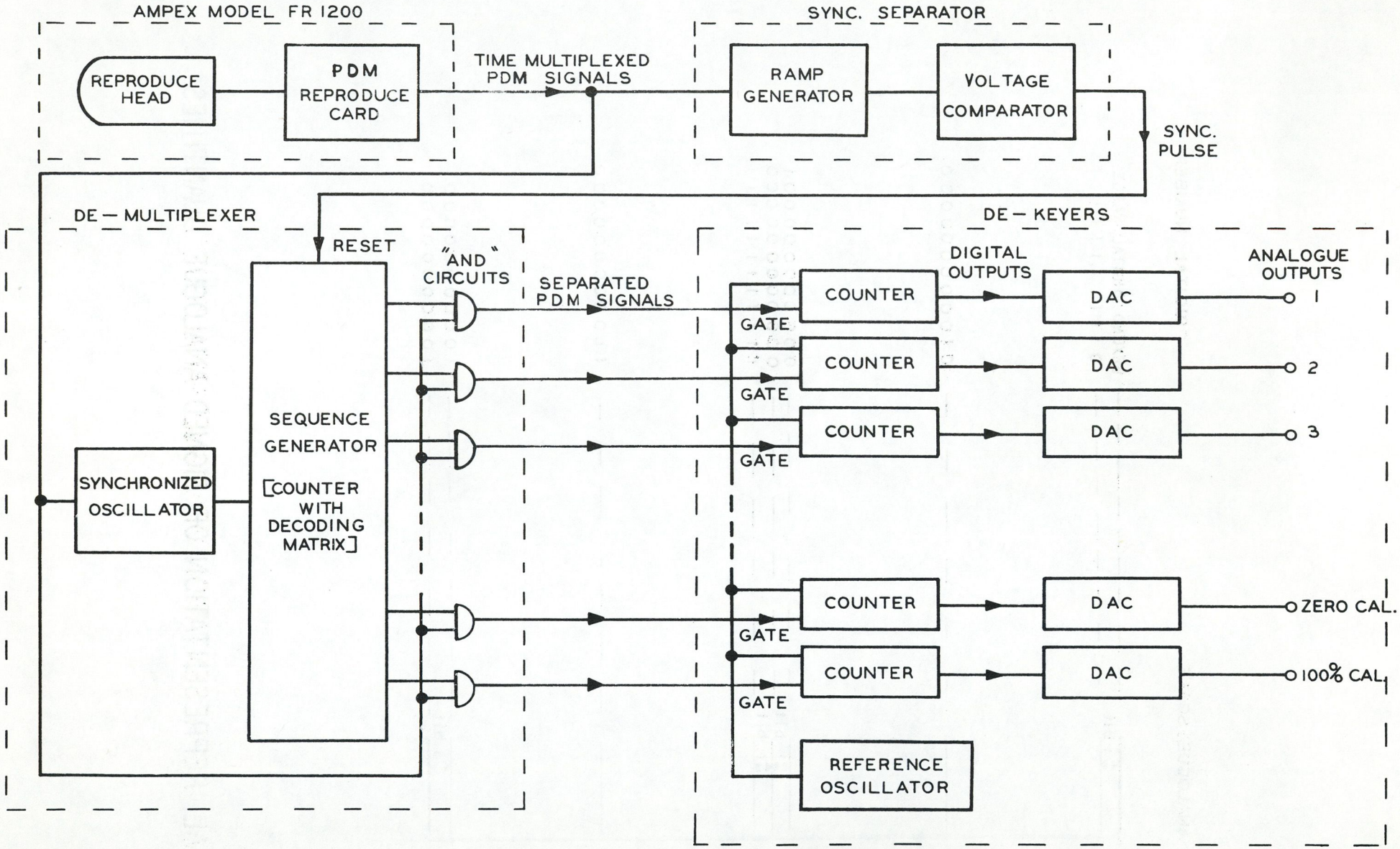
PROPOSED SYSTEM OF FLUTTER COMPENSATION

REPORT M.E. 126
FIG. 9



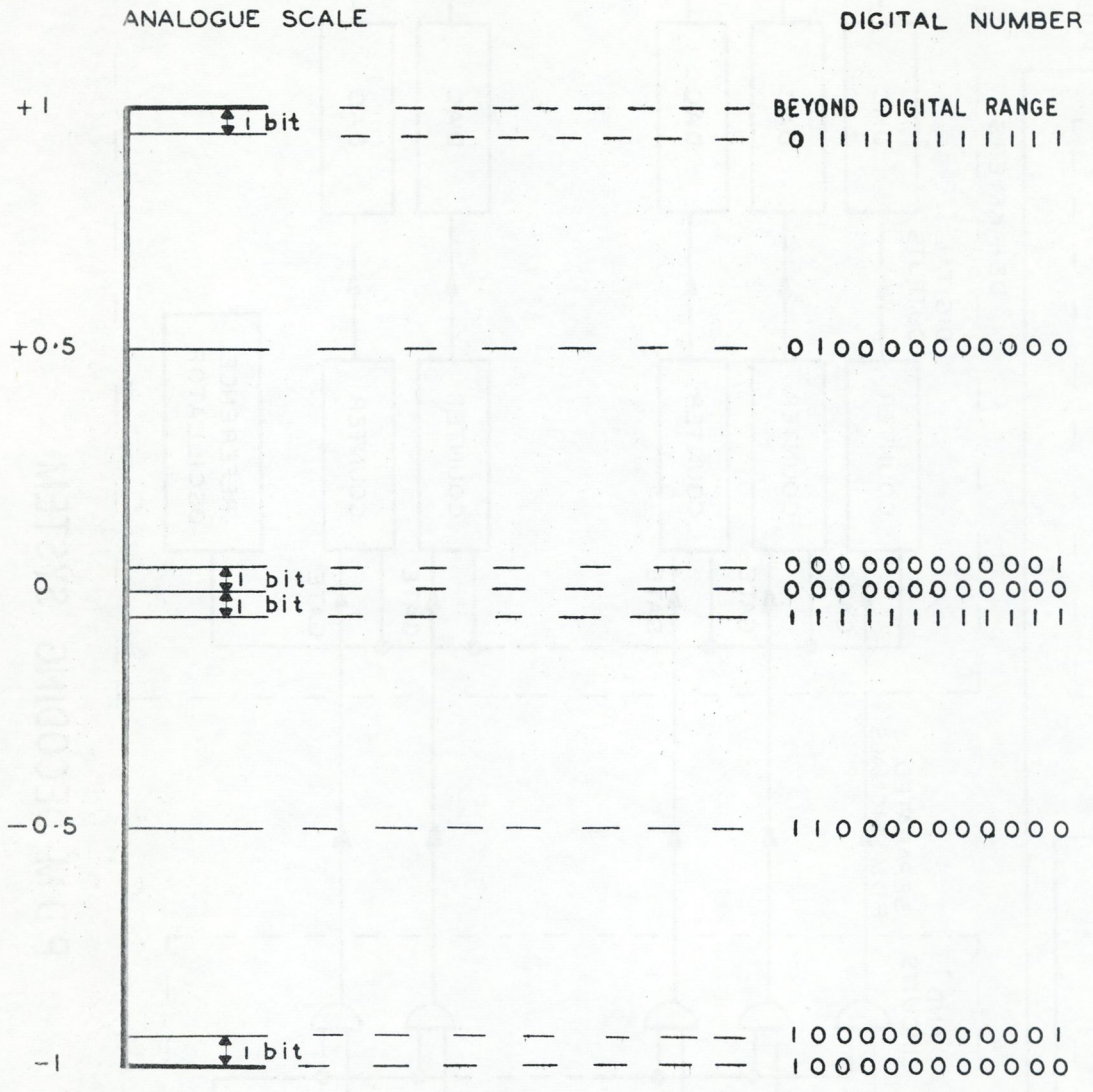
PDM RECORD SYSTEM

REPORT M.E. 126
FIG. 10

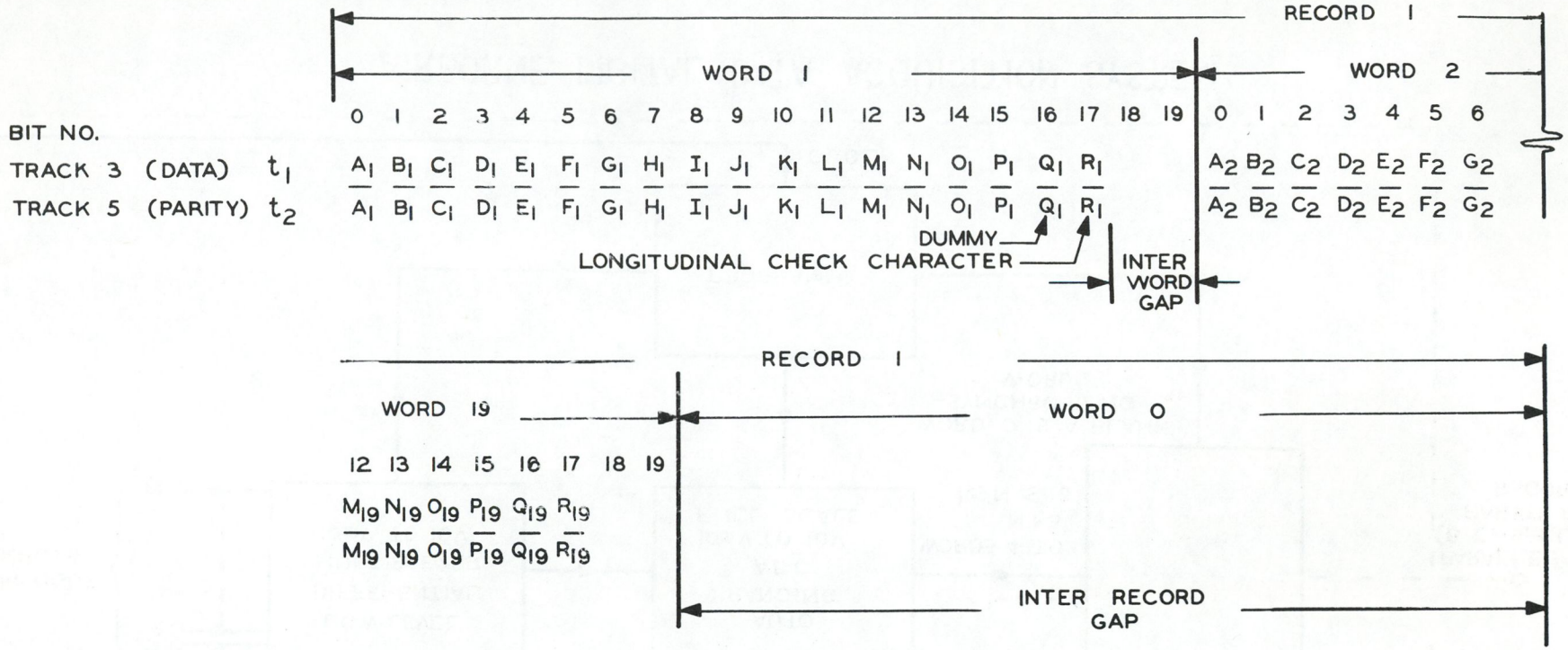


PDM DECODING SYSTEM

REPORT M.E.126
FIG. 11



DIGITAL REPRESENTATION OF SIGNED ANALOGUE QUANTITIES

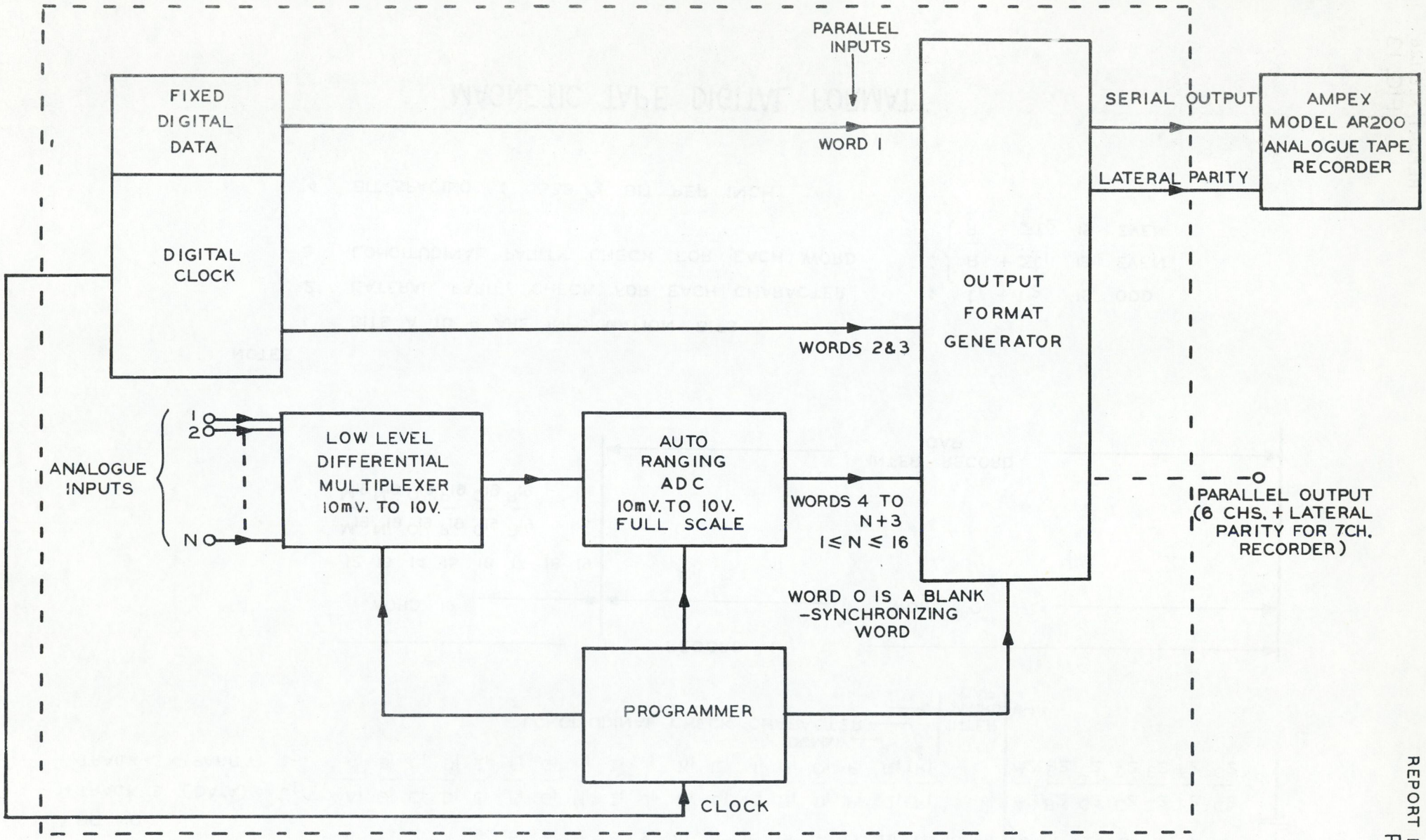


NOTES

1. BITS A TO P ARE INFORMATION BITS
2. LATERAL PARITY CHECK FOR EACH CHARACTER : $t_1 + t_2$ IS ODD
3. LONGITUDINAL PARITY CHECK FOR EACH WORD : $R + \Sigma t_1$ IS EVEN; $\overline{R} + \Sigma t_2$ IS EVEN
4. BIT SPACING : 333 1/3 BIT PER INCH

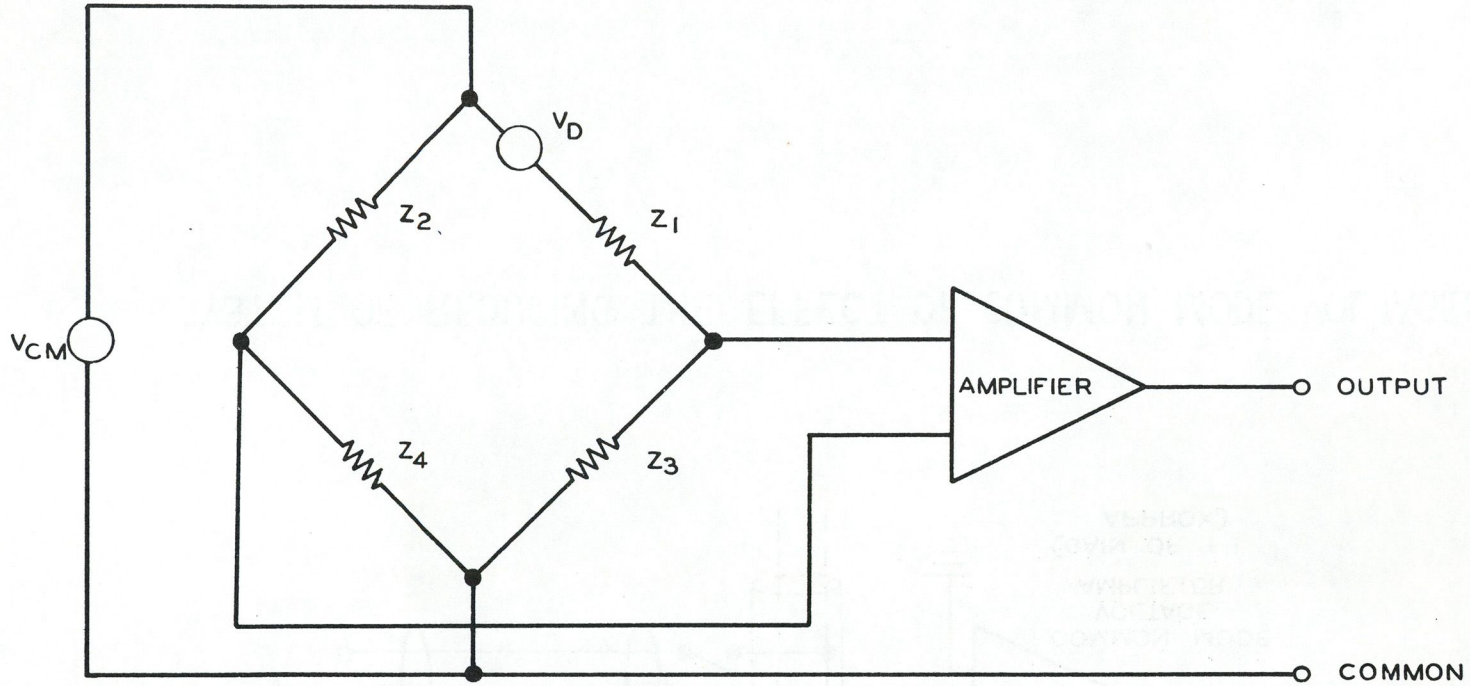
MAGNETIC TAPE DIGITAL FORMAT

REPORT M.E. 126
FIG. 13



AIRBORNE DIGITAL DATA ACQUISITION SYSTEM

REPORT M.E.126
FIG. 14

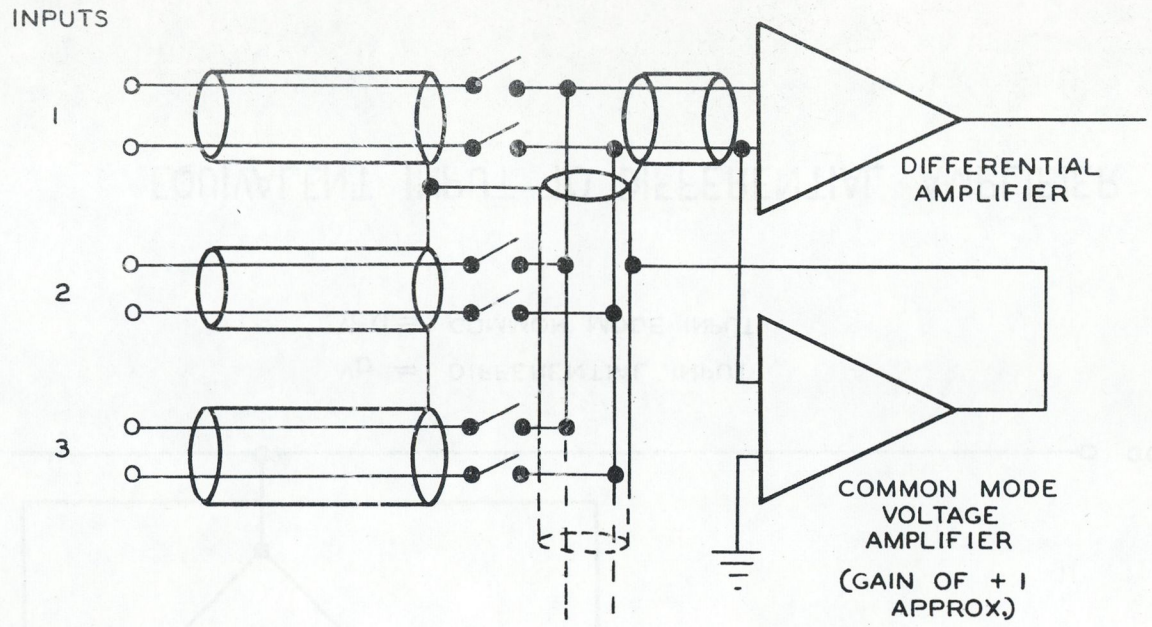


V_D = DIFFERENTIAL INPUT

V_{CM} = COMMON MODE INPUT

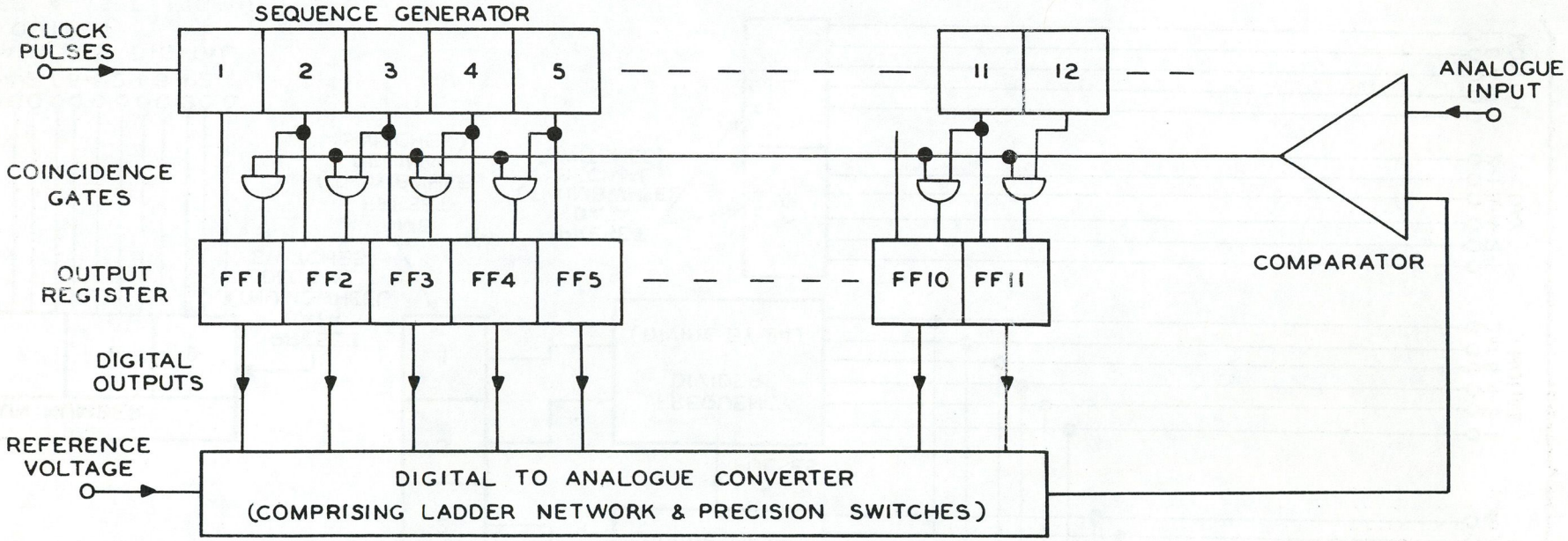
EQUIVALENT INPUT TO DIFFERENTIAL AMPLIFIER

REPORT M.E.126
FIG. 15



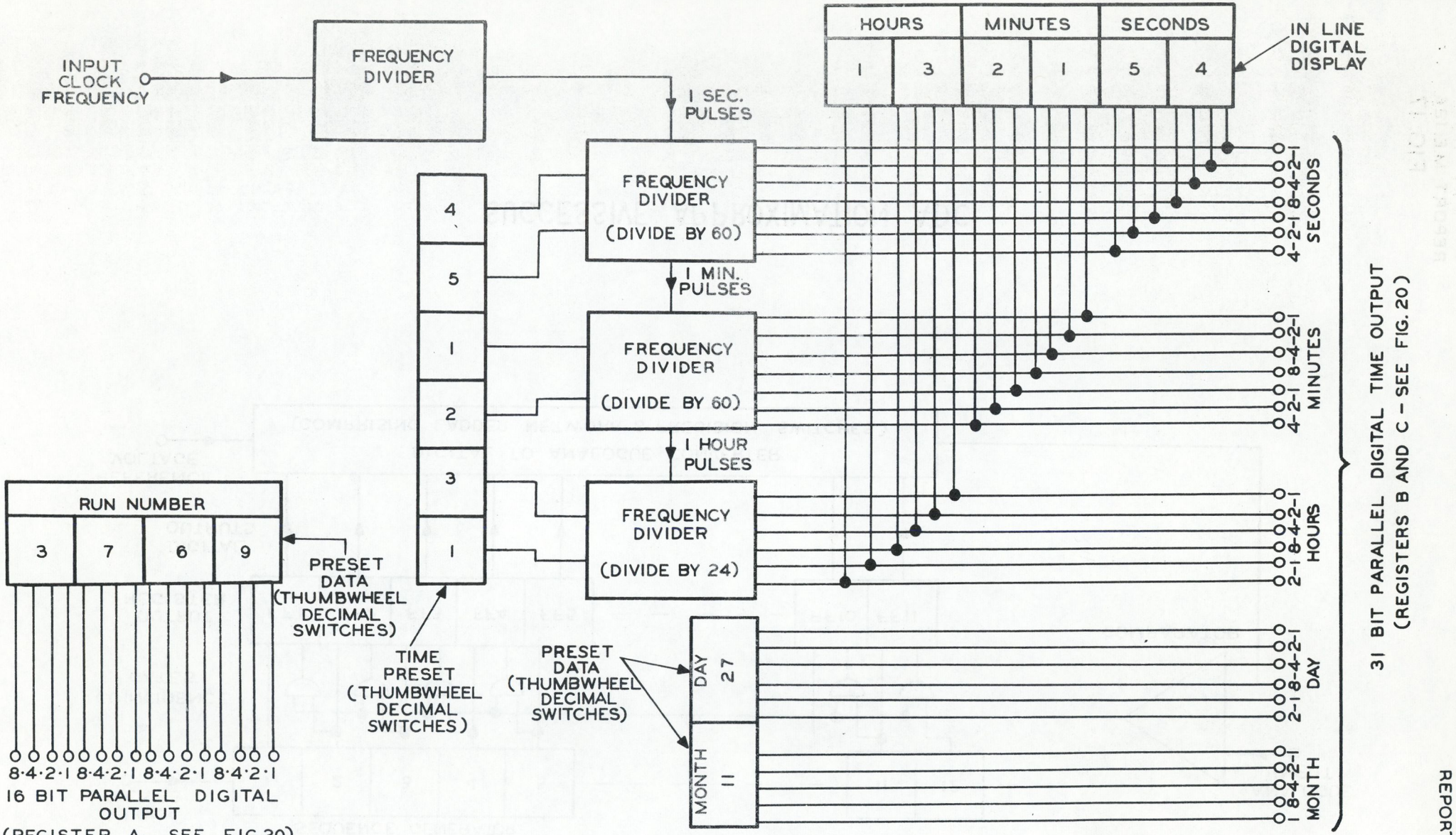
SYSTEM OF REDUCING THE EFFECT OF COMMON MODE VOLTAGES

REPORT M.E.126
FIG. 16



SUCCESSIVE APPROXIMATION ADC

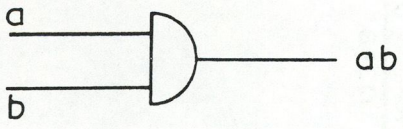
REPORT M.E. 126
FIG. 17



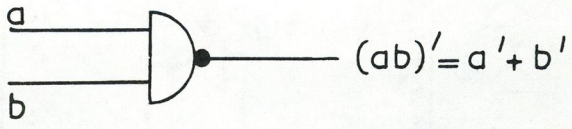
DIGITAL CLOCK

REPORT M.E. 126
FIG. 18

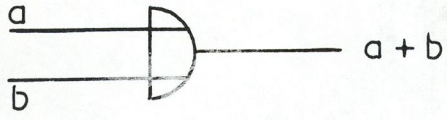
AND



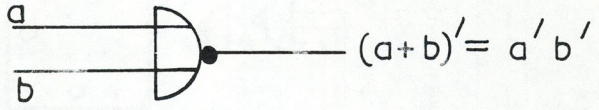
NAND



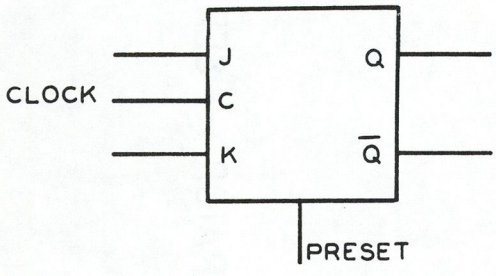
OR



NOR



J-K FLIP FLOP

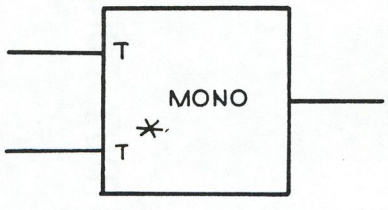


TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = BIT TIME BEFORE CLOCK PULSE

t_{n+1} = BIT TIME AFTER CLOCK PULSE

MONOSTABLE MULTIVIBRATOR



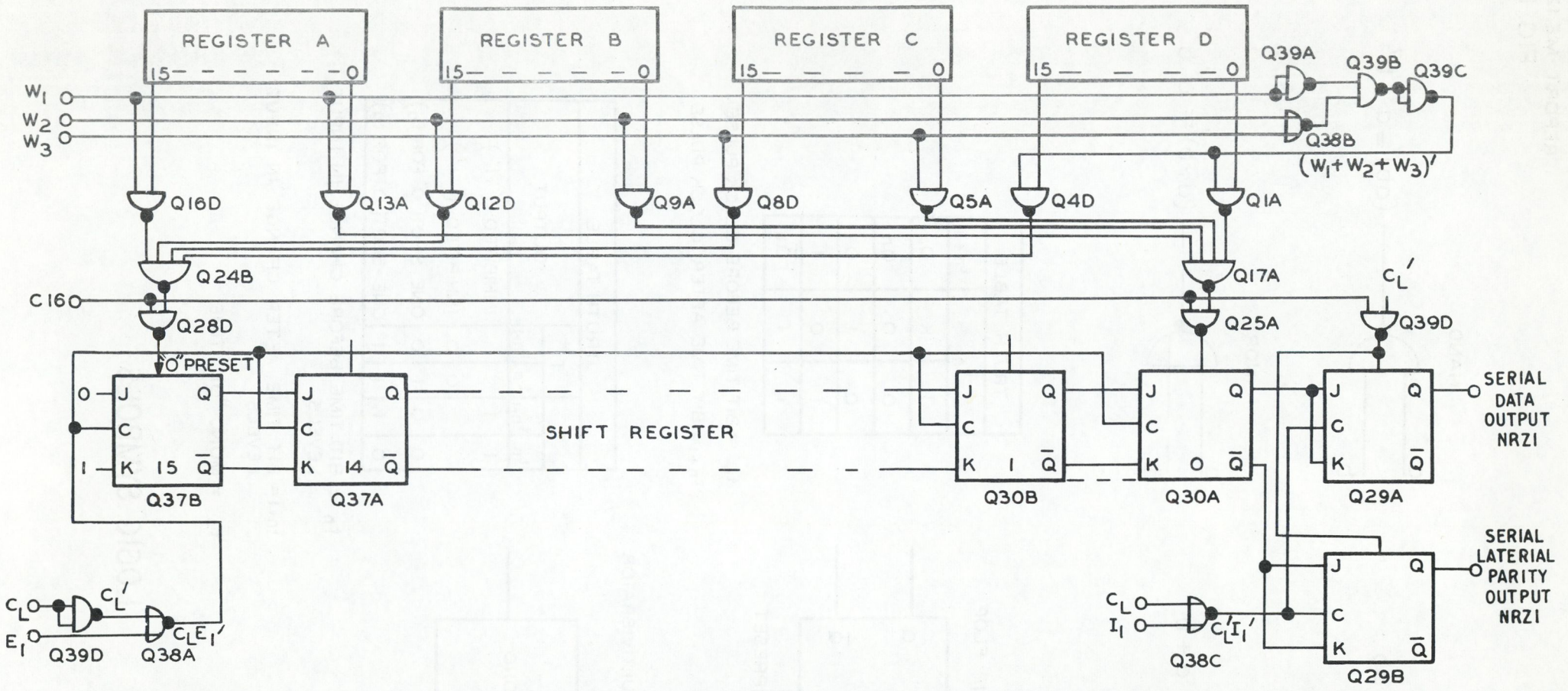
TRUTH TABLE				
T		T*		OUTPUT
t_n	t_{n+1}	t_n	t_{n+1}	
1	1			INHIBITED ("1")
		0	0	INHIBITED ("1")
0	0	1	0	ONE SHOT("0" FOR t_p)
0	1	1	1	ONE SHOT("0" FOR t_p)

t_n = BIT TIME BEFORE CHANGE IN INPUT LEVELS.

t_{n+1} = BIT TIME AFTER CHANGE IN INPUT LEVELS

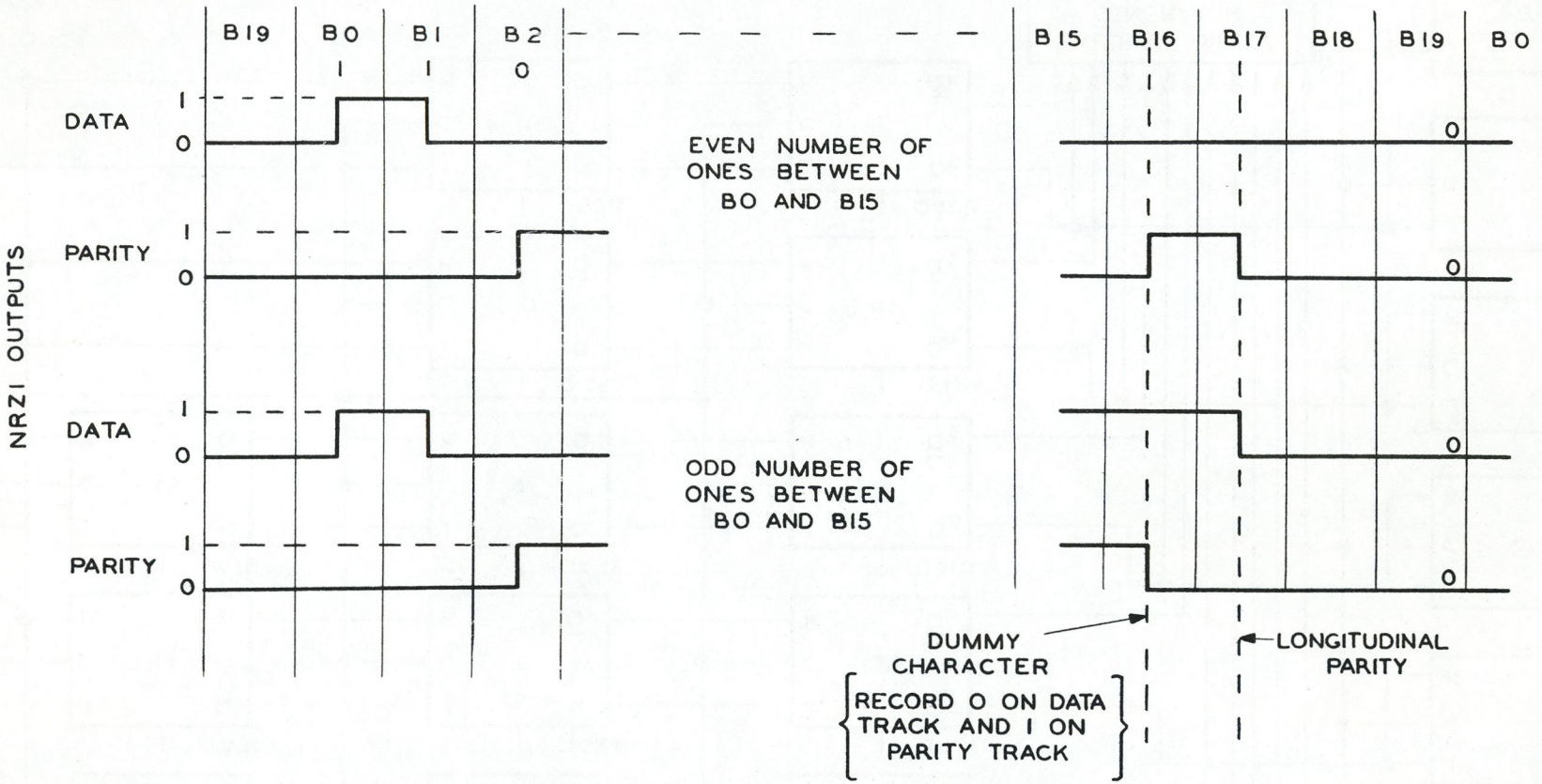
t_p = MONO "ON" TIME

LOGIC SYMBOLS



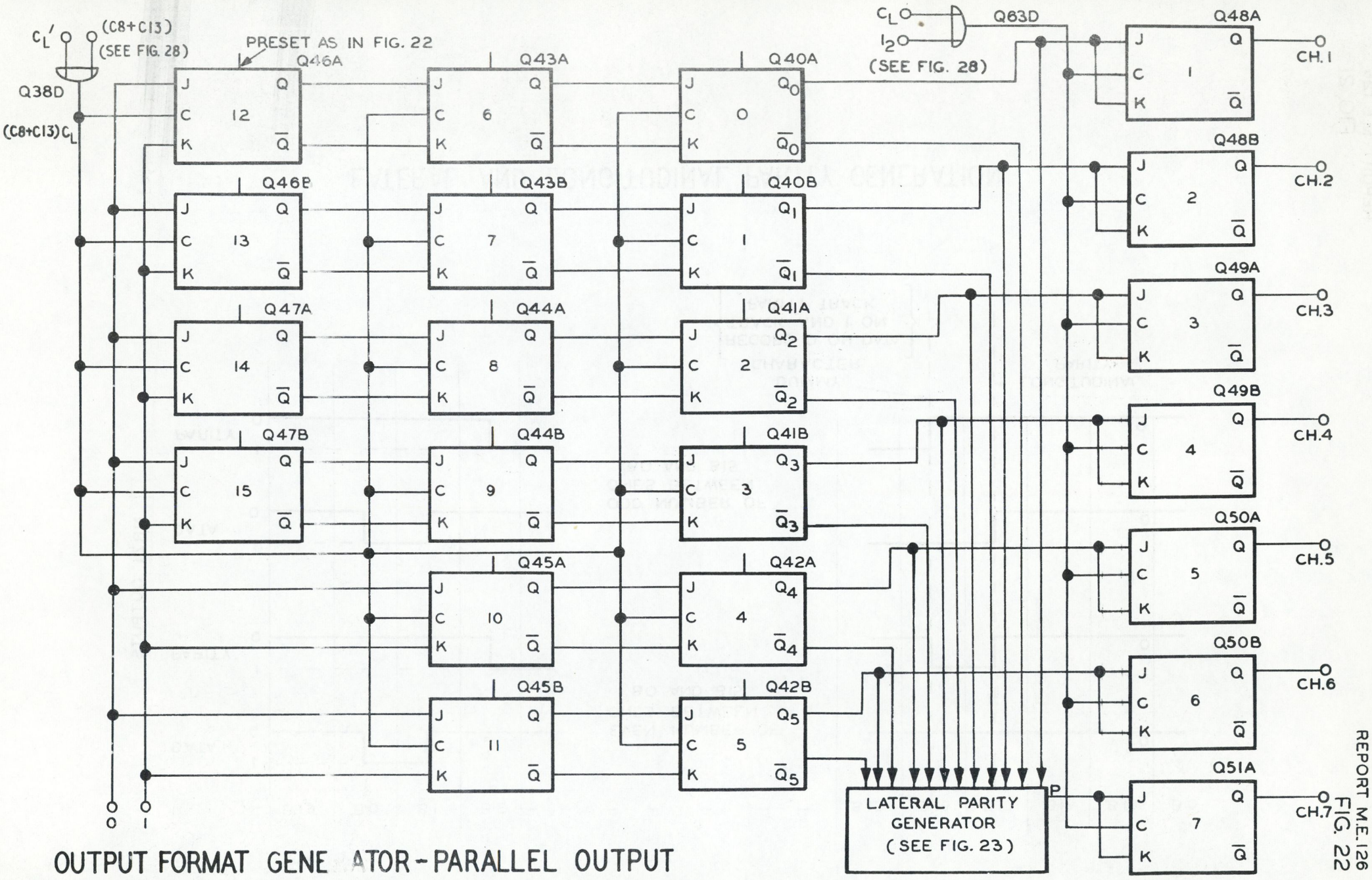
OUTPUT FORMAT GENERATOR — SERIAL OUTPUT

REPORT M.E. 126
FIG. 20



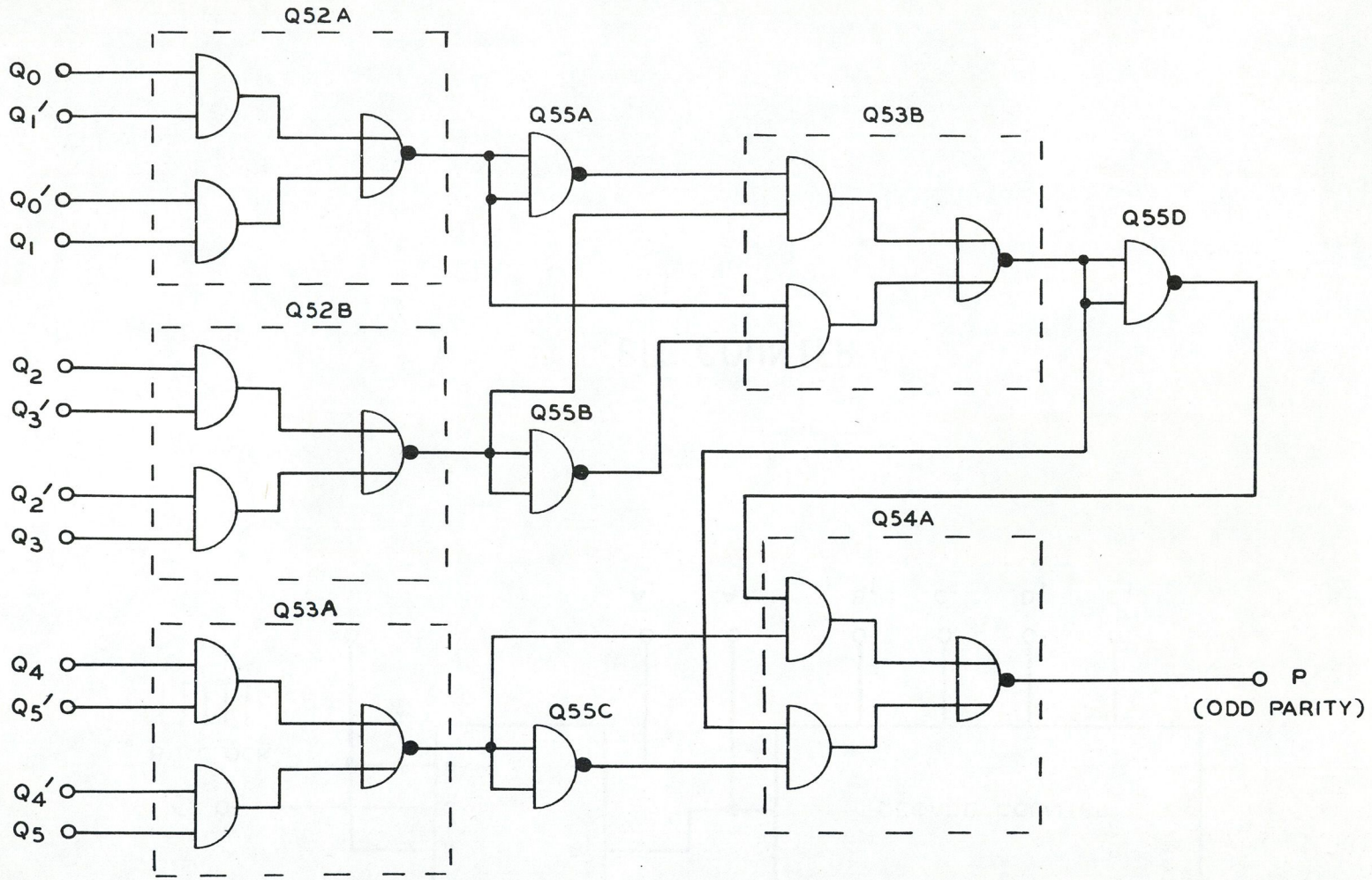
LATERAL AND LONGITUDINAL PARITY GENERATION

REPORT M.E.126
FIG. 21



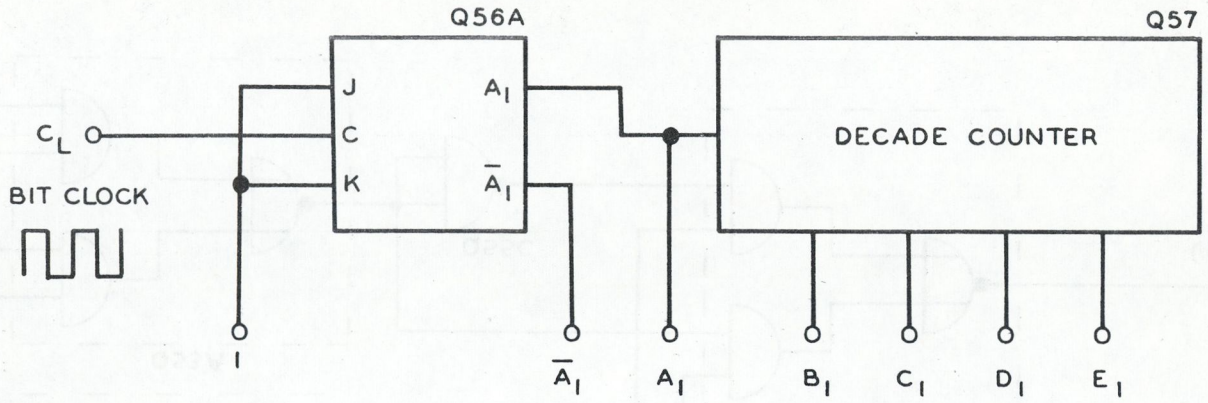
OUTPUT FORMAT GENE ATOR - PARALLEL OUTPUT

REPORT M.E.126 FIG. 22



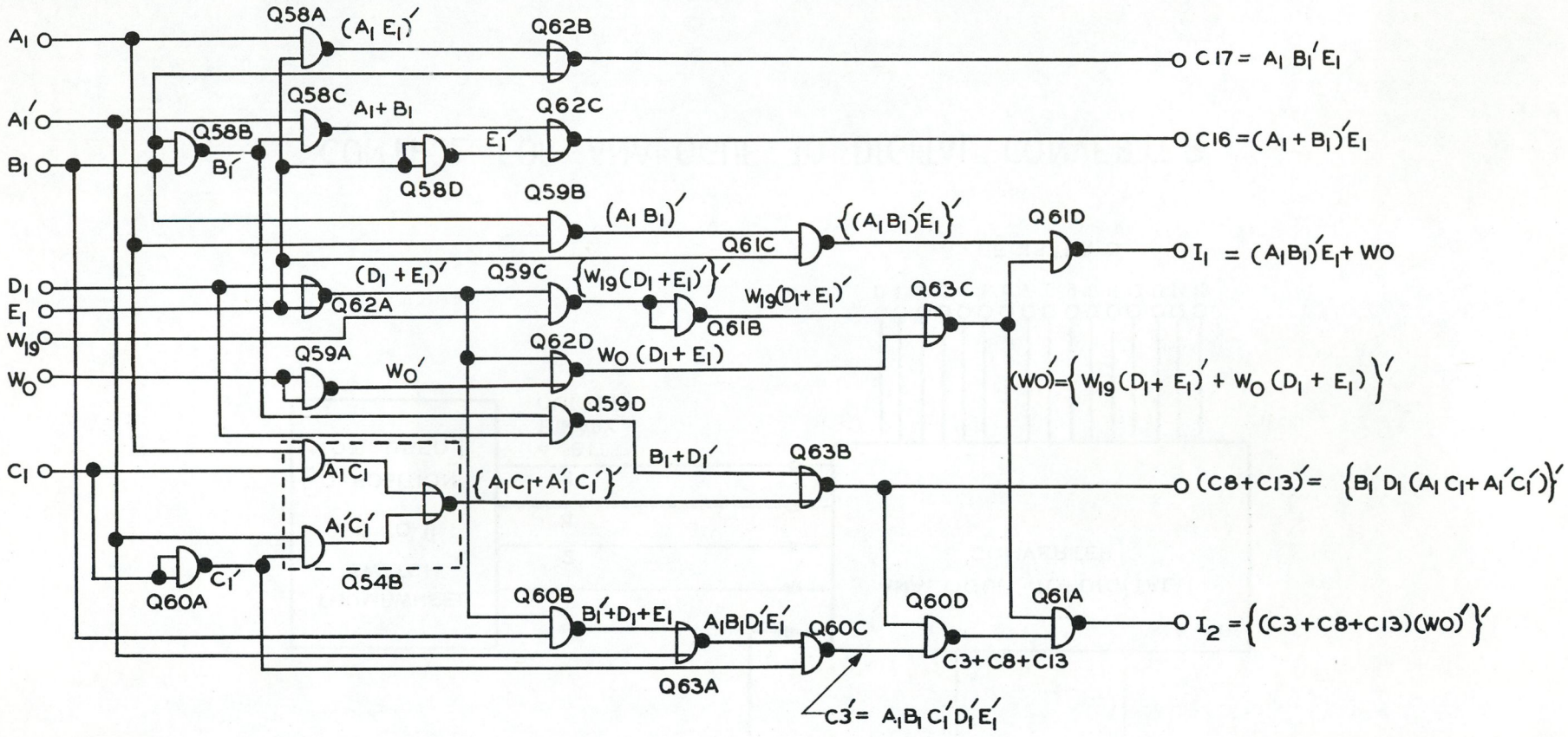
LATERAL PARITY GENERATOR

REPORT M.E.126
FIG. 23



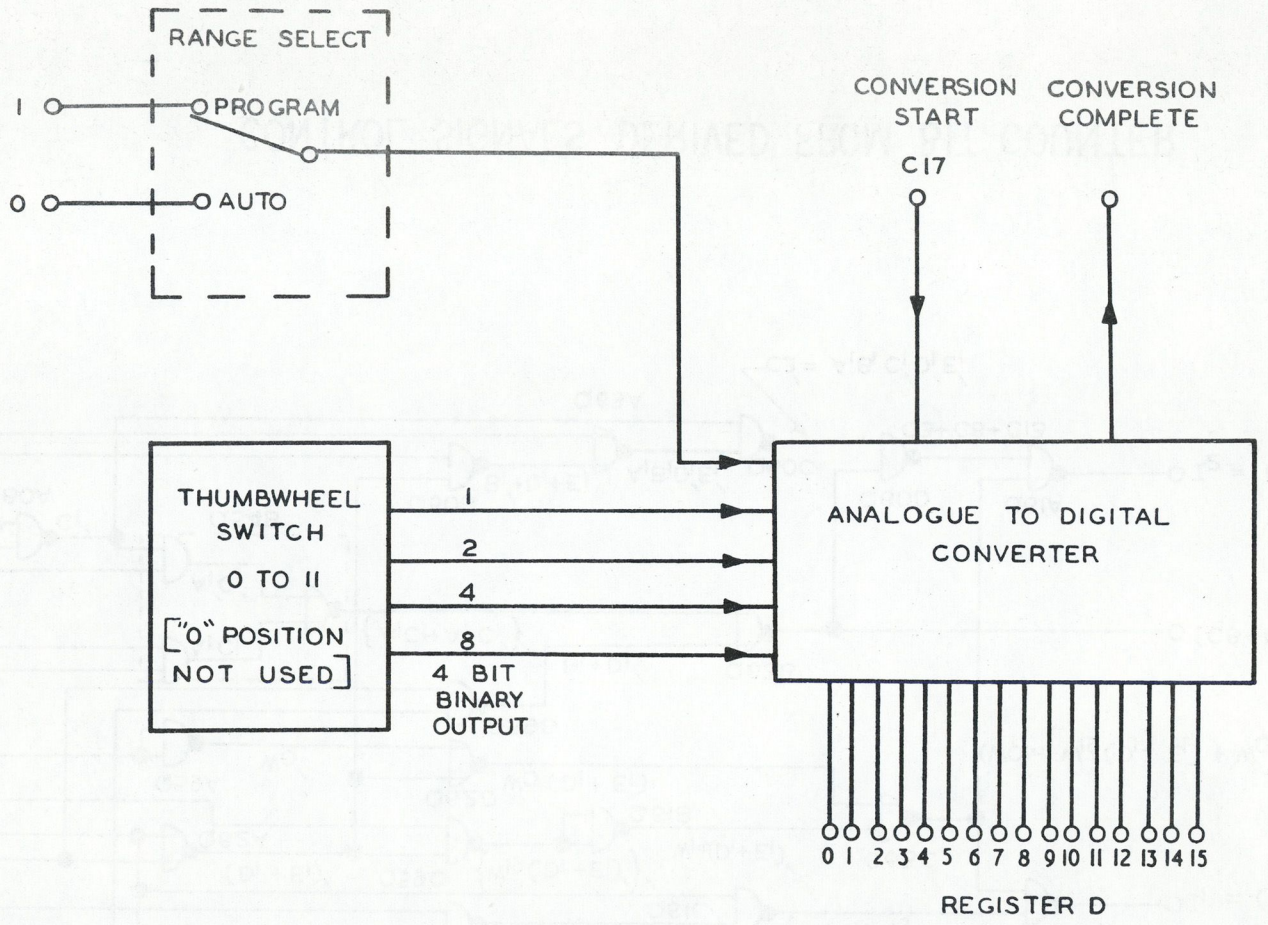
BIT COUNTER

REPORT M.E. 126
FIG. 24



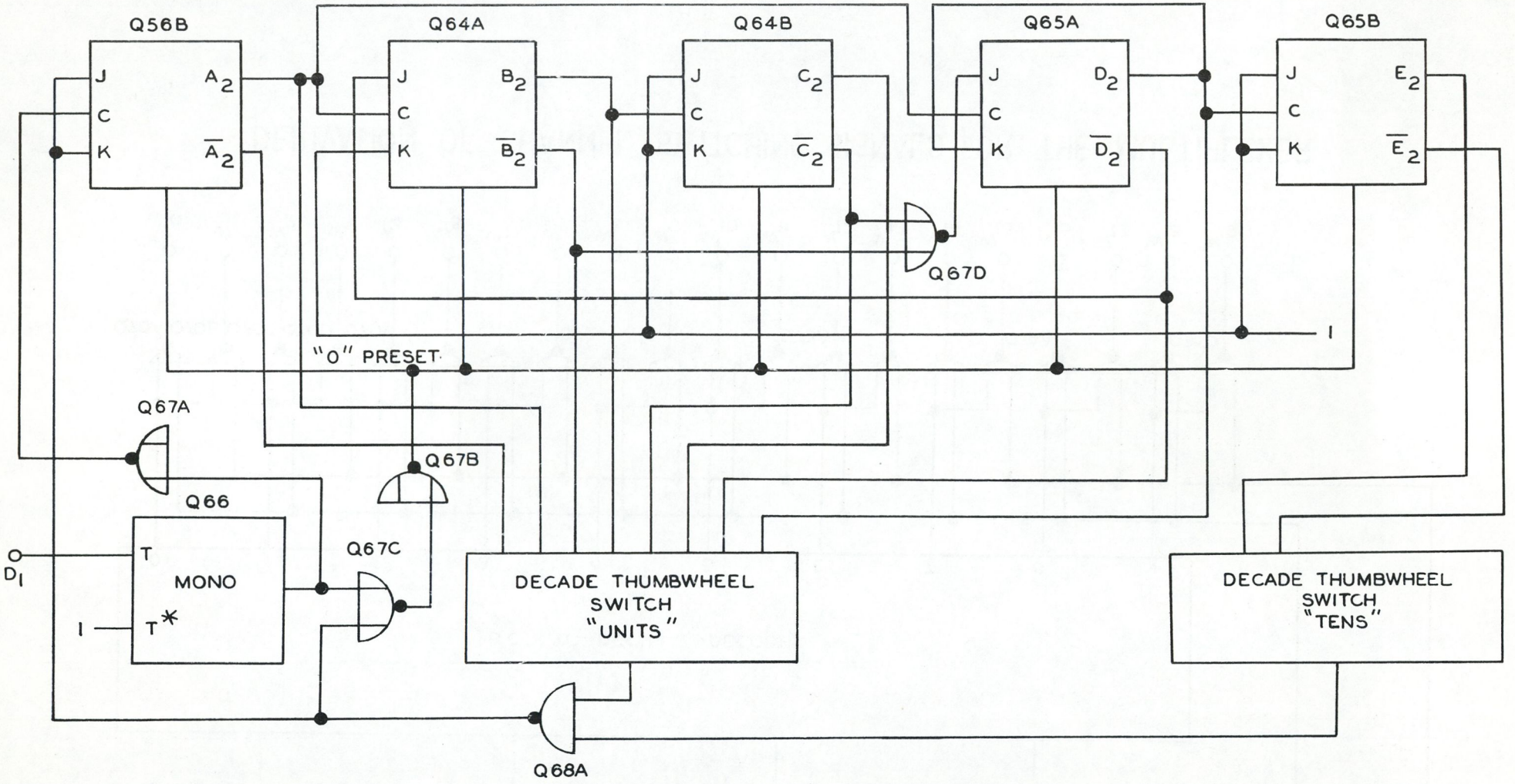
CONTROL SIGNALS DERIVED FROM BIT COUNTER

REPORT M.E. 126
FIG. 25



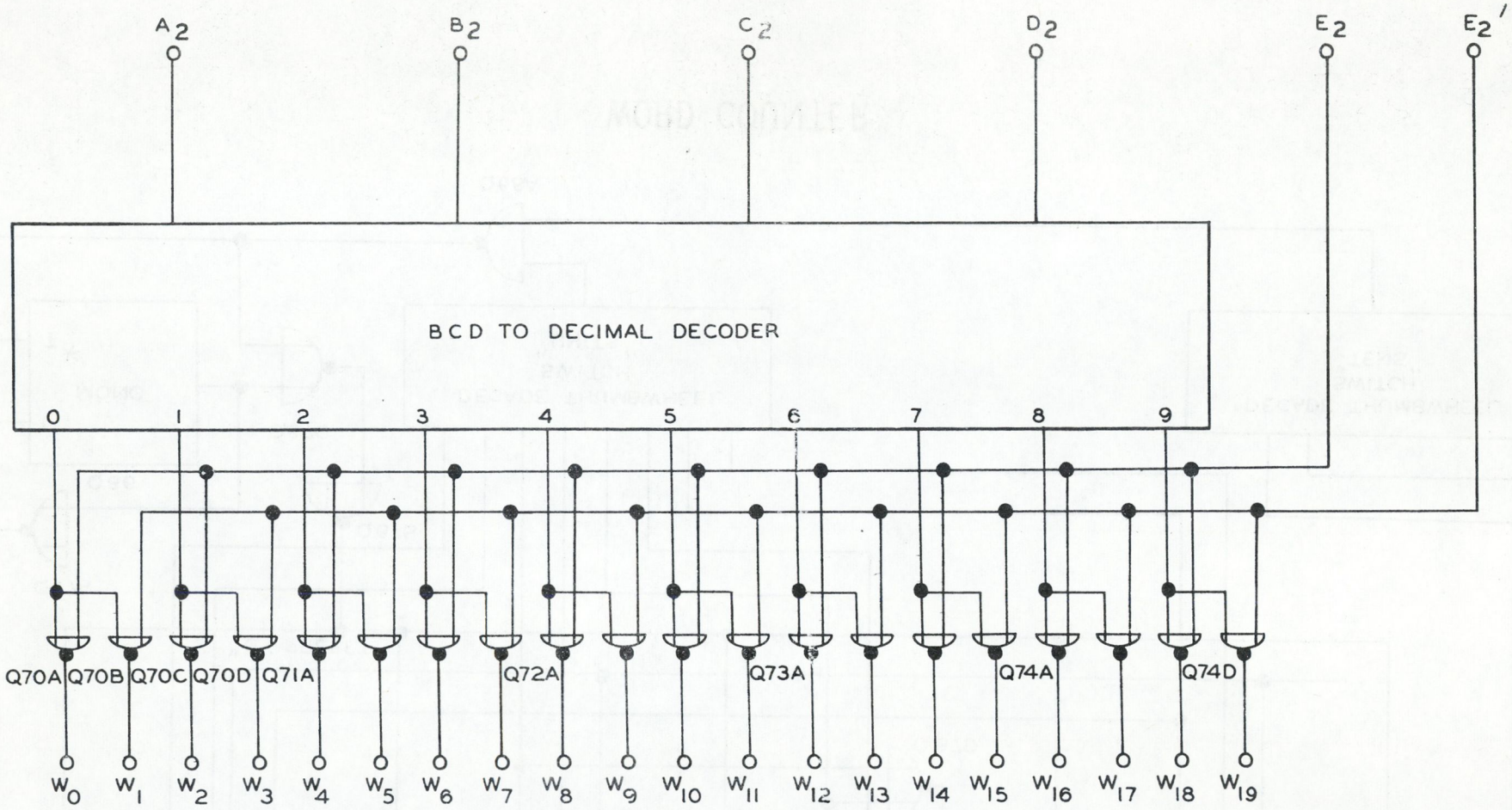
CONTROL FOR ANALOGUE TO DIGITAL CONVERTER

REPORT M.E. 126
FIG. 26



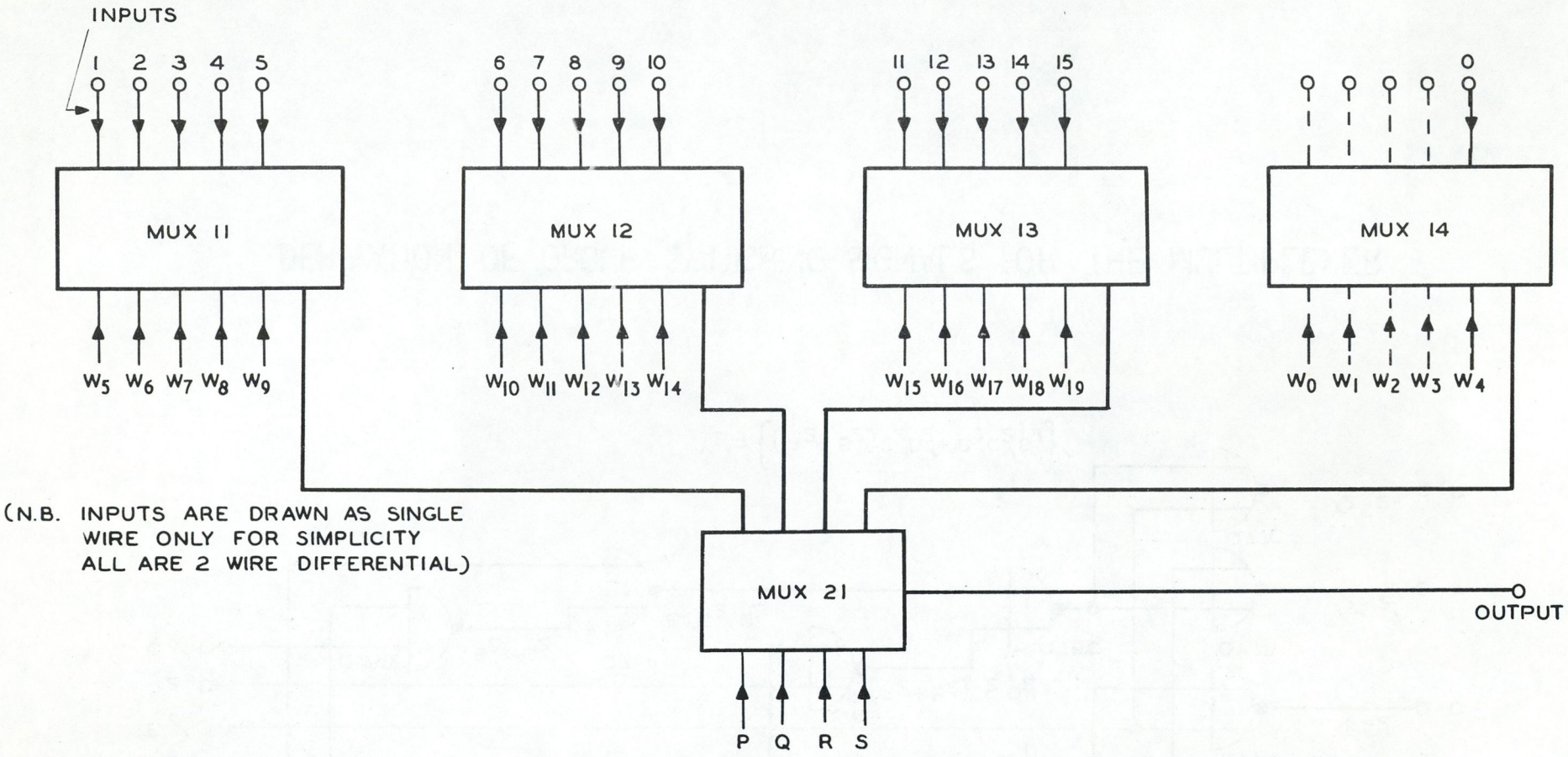
WORD COUNTER

REPORT M.E. 126
FIG. 27



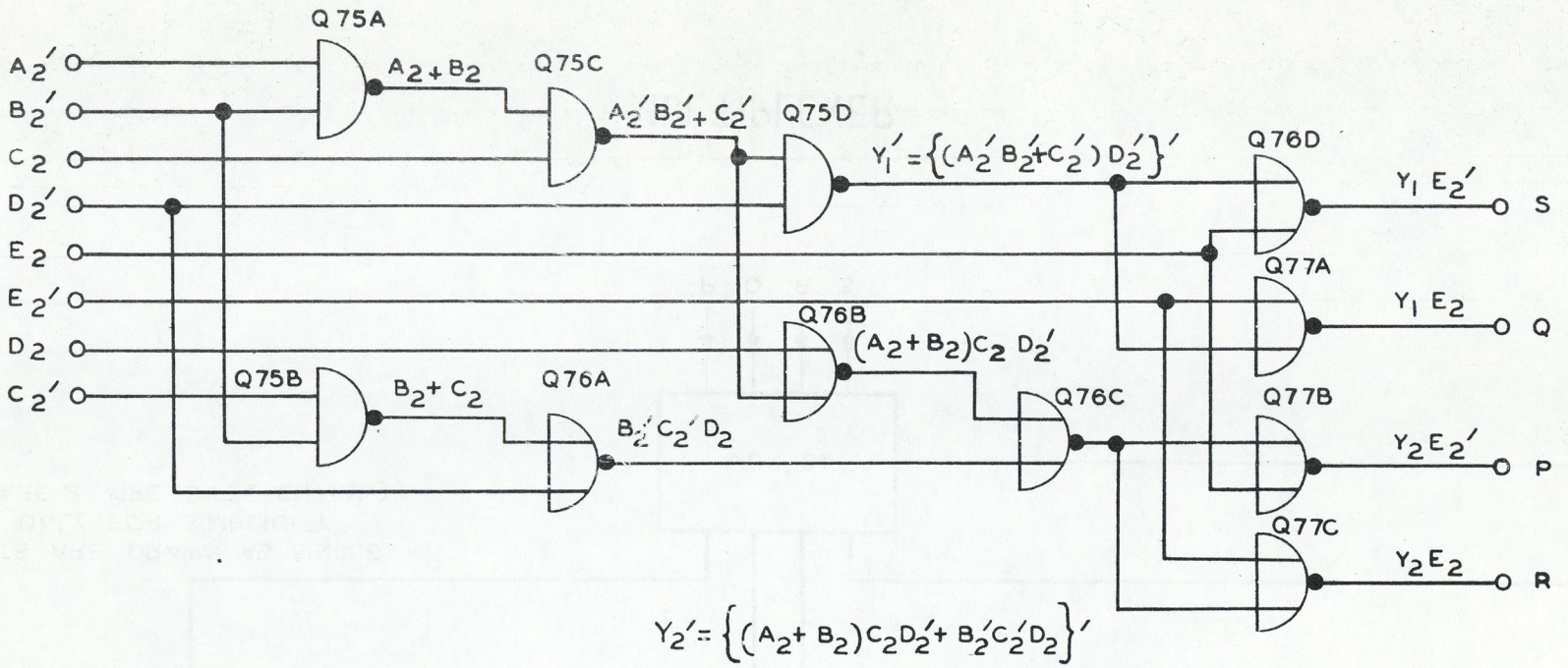
DERIVATION OF CHANNEL SWITCHING SIGNALS FOR THE MULTIPLEXER

REPORT ME. 126
FIG. 28



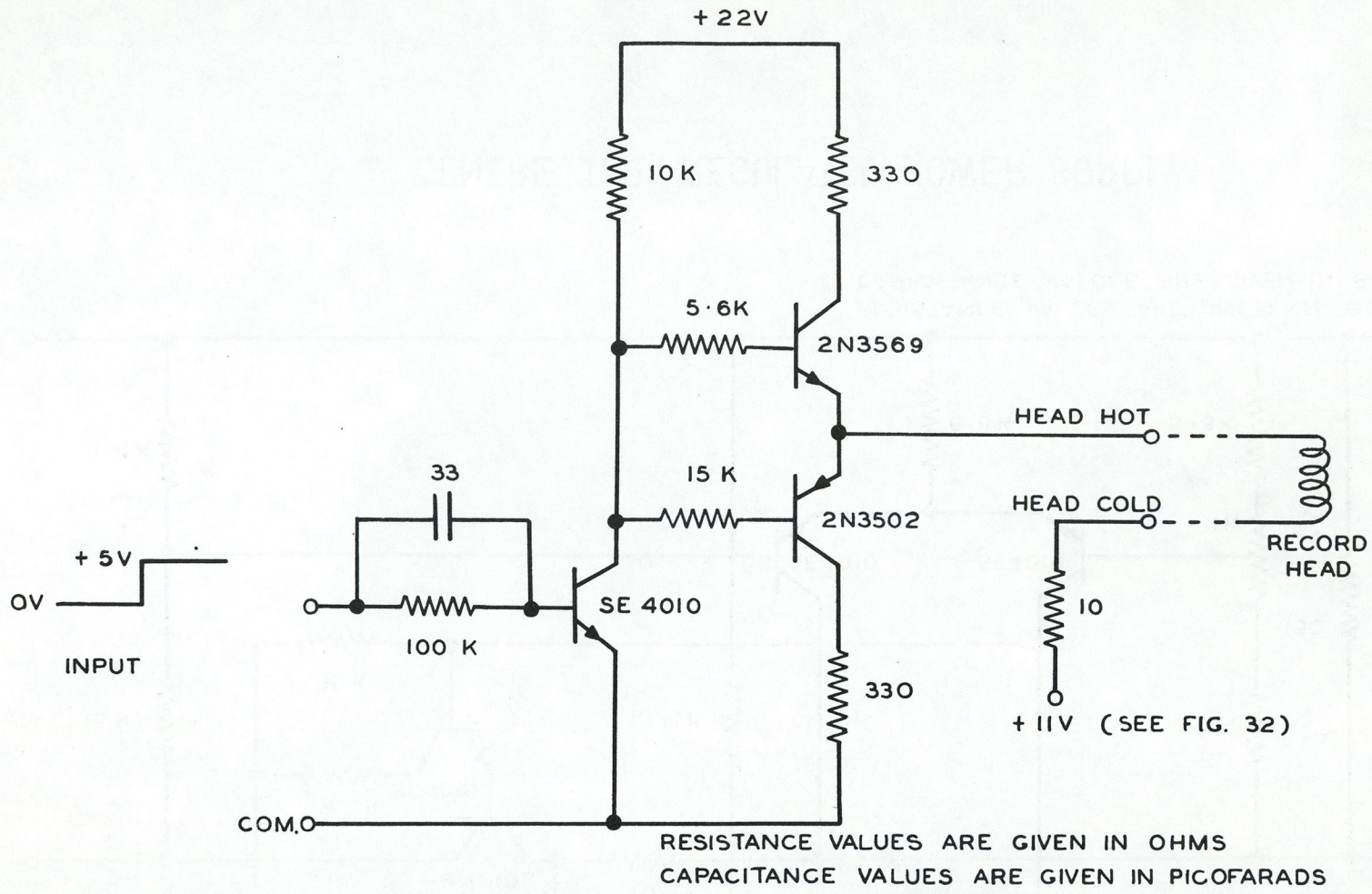
MULTIPLEXER

REPORT M.E.126
FIG. 29



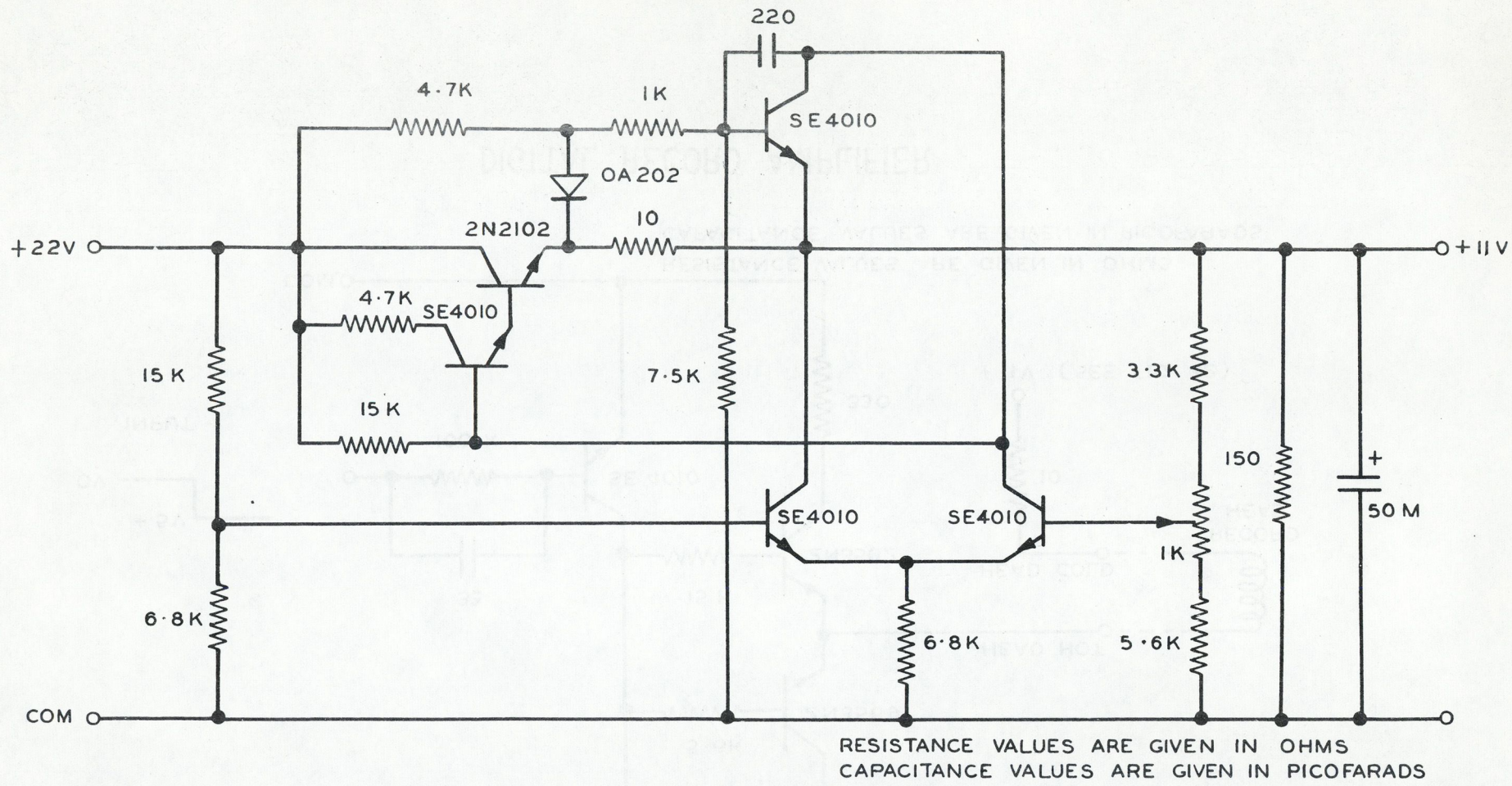
DERIVATION OF GROUP SWITCHING SIGNALS FOR THE MULTIPLEXER

REPORT M.E.126
FIG. 30



DIGITAL RECORD AMPLIFIER

REPORT M.E.126
FIG. 31



CENTRE TAP REGULATED POWER SUPPLY

REPORT M.E.126
FIG. 32