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GROUND STATION DIGITAL INTERFACE

by

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SUMMARY

Digital computer interface equipment has been developed to enable the recovery of digital data encoded in special format and recorded, both in flight and in laboratory experiments, using an analogue magnetic tape transport.

The recorded data are first reproduced, in a continuous manner, at the ground station processing centre, using an analogue magnetic tape reproducing machine and are then taken to the input of the interface equipment. Serial to parallel conversion of the data into 16-bit words suitable for direct entry into a computer, under interrupt control, is performed by the interface equipment.

Time-of-day information which is normally multiplexed with other digital data and recorded on the magnetic tape, effectively constitutes an identifier which may be used for specifying the location of any areas of interest on the tape. To enable the analogue reproducing machine to be stopped at any predetermined location, a preset stop signal generator has been incorporated in the interface equipment.

Complete details, together with a functional description, of each circuit within the digital interface equipment are included.

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16. *ABSTRACT*

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Time-of-day information which is normally multiplexed with other digital data and recorded on the magnetic tape, effectively constitutes an identifier which may be used for specifying the location of any areas of interest on the tape. To enable the analogue reproducing machine to be stopped at any predetermined location, a preset stop signal generator has been incorporated in the interface equipment.

Complete details, together with a functional description, of each circuit within the digital interface equipment are included.

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1. INTRODUCTION

In-flight data acquisition is an essential requirement for aircraft performance studies. In a system for airborne data logging[1,2] adopted at these laboratories the acquired data are stored on magnetic tape using a seven-track airborne analogue tape machine. Detailed analysis of the data is performed later with the aid of suitable ground station data reduction equipment.

Aircraft evaluation studies involve the measurement of many physical quantities. Some quantities such as vibration displacement, noise and pressures at various points in jet engines are not normally required to be measured with extreme accuracy but frequently involve measurement over large bandwidths. Such data are normally recorded using analogue techniques. Other quantities such as airspeed, altitude, air temperature and engine speed frequently have to be measured with very high precision but usually over a relatively small bandwidth. High precision is required to enable basic computed quantities such as Mach Number and True Air Speed to be accurately evaluated and to enable small changes in performance to be indicated. Digital techniques must be employed for the recording of such data to the desired accuracy. Fortunately, in aircraft studies, large bandwidth and high precision are very rarely required simultaneously in a given measurement.

Because of space limitations on smaller aircraft, particularly military types, a system of recording both analogue and digital information simultaneously using a single analogue tape machine has been evolved.[1,2]

Ground station equipment to process the data recorded using digital techniques comprises an analogue magnetic tape reproducing machine, a digital computer with suitable peripherals, and a special interface (which is the subject of this report) between the tape reproducer and the computer.

Correlation between data recorded using analogue techniques and data recorded using digital techniques is an essential requirement of the data reduction system. For instance there may be a requirement for correlating a vibration level (deduced from data recorded using analogue techniques) with Mach number (computed from a number of parameters recorded using digital techniques). Time-of-day information (multiplexed and recorded together with other digital data) provides a basic indentifier which enables data reduced at different times (with different equipment possibly) to be correlated in time.

The recorded time-of-day signal may be used in conjunction with a preset stop signal generator to stop the tape reproducing machine at any preset time. Such a system is incorporated in the interface.

General operating principles of the ground station interface were detailed[3] at an earlier stage in the development programme. However, since then some updating of the requirements and the circuits has occurred.

This report is one of a series describing equipment developed at these laboratories for use in airborne data acquisition and ground station data reduction applications.

2. GENERAL DESCRIPTION

The recorded digital data[1,2] may be in either serial form (on one or two tracks depending on the method of encoding) or parallel form (on seven tracks). Up to the present only serial recording has been performed but both the data acquisition equipment and the data reduction equipment have been designed to accommodate the parallel recording. The parallel system would be considered only when large quantities of digital information (but no wideband analogue information) have to be recorded.

Neither the serial nor the parallel forms of recording considered here produce a computer compatible tape and hence the tapes cannot be read directly into a digital computer using a conventional magnetic tape interface.

At present either of two alternative systems of encoding the digital data may be employed for the serial system of recording. In the first system the data are encoded in NRZ (non-return-to-zero) form on two tape tracks. A NRZM (non-return-to-zero-mark) signal is recorded on one track and a NRZS (non-return-to-zero-space) signal recorded on another track. Recording of the data in this manner allows a clock signal to be re-introduced when the data are reproduced. In the second system the data are encoded in RZ (return-to-zero) code which is self clocking and requires only one tape track.

It is appreciated that the Bi-phase[4] coding (often referred to as Phase Encoding) can be used for recording the data using a single tape track, as a clock signal can be re-introduced when the data are reproduced (as for the RZ data). However, the RZ format[5] provides a signal for which a clock signal may be generated very simply over a wide range of tape speeds using flywheel techniques. The simplicity results because recorded ones and zeros yield the same signal frequency when the data are reproduced. In contrast recorded ones yield twice the signal frequency that recorded zeros yield if phase encoding is used.

When the serial system is used, digital reproducing amplifiers[5] generate a two-line output (comprising a NRZM and a NRZS signal) as illustrated in Figure 1. When the parallel system is used, a seven-line output is generated using NRZM code.

In both cases the outputs may be coupled directly to the input of the digital interface.

For data recorded serially[1,2] each word is composed of 16 information bits (in some cases the effective words are shorter and unused bits are recorded as zeros), one longitudinal parity bit, one dummy bit and a space of two-bit durations constituting an end-of-word (EOW) gap. The number of words per data frame (or record) may be set in the range 2 to 104 by the recording equipment. At present the recording equipment will accommodate 32 channels of multiplexed analogue data (subsequently converted to digital form with an analogue to digital converter) and hence the upper limit generally does not exceed 35 channels after due allowance for three digital inputs providing time-of-day and other information.

Each data frame is followed by an end-of-record (EOR) gap having a duration equivalent to that of one word plus an EOW gap. Hence a data gap of effectively 22-bit duration occurs at the end of each data frame. To read the reproduced digital data it is essential that the interface equipment detect both EOW and EOR gaps.

An EOW gap (Fig. 1) is characterized by no level change on either the NRZM input (referred to subsequently as the NRZ1 input) or the NRZS input (referred to subsequently as the NRZ2 input).

It was originally envisaged that an EOR gap would be characterized by a similar no-level change and to this end a serial digital data generator,[6] which incorporates such a system of frame synchronization and which provides signals of standard word composition for checking the ground station digital interface, has been manufactured. However, more recently, a system[2] of frame synchronization has been incorporated in the airborne data processor for which some level changes are recorded during the EOR gap. The earlier system of frame synchronization will be referred to as "Type A" and the more recent one as "Type B". These alternative systems are illustrated in Figures 2 and 3. Both forms of frame synchronization are recognized by the interface.

For the serial system of digital recording a word rate of 1024 per second is used for data recorded at 152·4 cm/s [60 ips (inches per second)] tape speed. Proportionately lower word rates are used at lower tape speeds.

The interface will read incoming digital data reproduced at any tape speed within the range 4·76 cm/s ($1\frac{7}{8}$ ips) to 152·4 cm/s (60 ips). The number of data frames (records) reproduced per second at a tape speed of 4·76 cm/s is indicated in the following table as a function of the number of words in each record.

Words per record	1	4	5	8	10	16	20
Records per second (at 4·76 cm/s tape speed)	32	8	6·4 (32 per 5 sec.)	4	3·2 (16 per 5 sec.)	2	1·6 (8 per 5 sec.)

For parallel digital recording (seven-track) NRZM code is used on each track. Data are recorded on four tracks (say tracks 1 to 4), word and frame synchronizing signals are recorded respectively on tracks 5 and 6, and odd lateral parity checkbits are recorded on track 7. Hence four longitudinal bit groups (or bytes) are used to record one data word. The recording format which has been adopted is indicated in the following table.

Interface input	Encoded data											
NRZ1	b_0	b_4	b_8	b_{12}	b_0	b_4	b_8	b_{12}	b_0	b_4	b_8	b_{12}
NRZ2	b_1	b_5	b_9	b_{13}	b_1	b_5	b_9	b_{13}	b_1	b_5	b_9	b_{13}
NRZ3	b_2	b_6	b_{10}	b_{14}	b_2	b_6	b_{10}	b_{14}	b_2	b_6	b_{10}	b_{14}
NRZ4	b_3	b_7	b_{11}	b_{15}	b_3	b_7	b_{11}	b_{15}	b_3	b_7	b_{11}	b_{15}
NRZ5	0	0	1	1	0	0	1	1	0	0	1	1
NRZ6	1	1	1	1	0	0	0	0	1	1	1	1
NRZ7	p	p	p	p	p	p	p	p	p	p	p	p
	Word period $\leftarrow W_{N_D+N_A}{}^* \rightarrow$				Word period $\leftarrow W_0 \rightarrow$				Word period $\leftarrow W_1 \rightarrow$			

W_0 is the word period corresponding to the frame synchronizing word as encoded.

Time-of-day and fixed information are encoded during word period W_1.

N_D is the number preset on the digital channels selector switch and N_A is the number preset on the analogue channels selector switch in the airborne data processor.[2]

Digital reproducing amplifiers (which plug into the analogue reproducing machine) generate a seven-line digital input (designated NRZ1 to NRZ7) in NRZM code which is coupled to the interface.

"p" in the above table signifies an odd parity checkbit i.e. (if the sum of the binary digits encoded on NRZ1 to NRZ6 is even a "1" is encoded on NRZ7).

The data encoded on NRZ6 is the inverse of that which had been indicated previously.[3]

A data processor[2] included in the airborne data acquisition equipment multiplexes the following digital signals into appropriate data streams as required for the serial and the parallel systems of recording respectively.

(i) Output (16-line) of an airborne analogue to digital converter[2] which, with an associated analogue multiplexer, allows time multiplexing of up to 32 channels of data.

(ii) A time-of-day signal (20-line) from a time code generator included in the data processor.

(iii) Fixed data (27-line) comprising run number, day-of-the-month, and month-of-the-year information (all of which may be preset via thumbwheel switches mounted on the front panel of the data processor).

(iv) Outputs (up to two 16-line) from digital transducers or other devices.

The multiplexed digital data in NRZ code form the inputs to the interface.

Basically the digital interface is required to:

(i) arrange the digital data into 16-bit parallel words which may be conveniently read into a digital computer;

(ii) display run number, month-of-the-year, day-of-the-month and time-of-day information;

(iii) provide a control signal which will enable the analogue reproducing tape transport to be stopped at any preset time;

(iv) provide synchronizing signals which will allow time multiplexed data[2] recorded using FM (frequency modulation) techniques to be demultiplexed (via equipment external to the interface) under the control of the reproduced time-of-day signal.

The various functions performed by the digital interface are indicated in the block schema of Figure 4.

The digital interface is constructed in a standard rack format. All circuits except those associated with the front and the rear panels, and the power supply, are mounted on plug-in printed circuits. In the following table the various circuits incorporated in the interface are listed.

Board description	Card slot number
AC to DC Converter	not plug-in
Voltage Regulators	0
Output Buffers	1
Input Clock Signal Generator	2
Electronic Flywheel	3
Control Signal Generator for Serial System	4
Control Signal Generator for Parallel System*	5
Serial to Parallel Converter for Serial System	5
Serial to Parallel Converter for Parallel System*	5
Time-of-Day Store and Preset Stop Generator	6
Selected Data and Fixed Data Store	7
Computer Interrupt Controller	8

* Boards for the serial system are replaced with boards for the parallel system in these cases.

The function of each of the printed circuit boards listed in the above table will be described in turn in the following sections.

Information on the system of component identification used in this report is given in Appendix 1. Additional system details required for circuit manufacture, operation and in-service maintenance are provided in another document[7] the contents of which are summarized in Appendix 2.

3. DETAILED CIRCUIT DESCRIPTIONS

3.1 AC to DC Converter

The digital interface requires regulated supplies of +5 V for digital circuits, +15 V and −15 V for the electronic flywheel circuit (Section 3.5), and an unregulated supply of nominally +180 V for use with neon numeric indicator tubes incorporated in front panel displays. Suitable DC outputs are generated by a conventional mains (240 V, 50 Hz) AC to DC converter using transformer, diode-bridge rectifiers and filter components.

Output voltages, indicated in Figure 5, are defined as follows:

V_C is the filtered voltage output from the high current low voltage supply which forms the input to the +5 V regulator (Section 3.2);

V_{CR} is the reference supply voltage output which is considerably higher than V_C but derived from the same transformer secondary winding output as the V_C supply;

V_A is the voltage output from the converter which forms the input to the +15 V regulator (Section 3.2);

V_B is the voltage output from the converter which forms the input to the −15 V regulator (Section 3.2);

V_D is the voltage output from the high voltage supply required for the indicator tubes. Typical performance figures for 240 V mains input are tabulated below.

Supply	Typical voltage/current	Ripple (peak to peak)
V_C	7·4 V at 3 A	400 mV
V_{CR}	25 V at 11 mA	4 V
V_A	18 V at 100 mA	1·5 V
V_B	−18 V at 100 mA	1·5 V
V_D	190 V at 42 mA	6 V

The equipment operates reliably for mains voltages between 220 and 250. For 240 V mains input, current drawn is 180 mA; thus power consumption is 43 W approximately.

An L-C type filter (Fig. 5) is employed for the generation of the V_C output. A form of voltage multiplier is used to generate the V_{CR} voltage output for use with the integrated circuit regulating device (Section 3.2) incorporated in the +5 V regulator.

Simple shunt capacitors provide filtering for the V_A, V_B and V_D supplies. Resistors R02, R03 and R04 are coupled to front panel indicator tube display switches. These resistors, which are switched in shunt across the V_D supply when the relevant portions of the front panel indicator tube displays are switched off, maintain the V_D output voltage approximately constant irrespective of which displays are "on". Excessive voltage, which could reduce the life of the indicator tubes, is therefore avoided.

The AC to DC converter is assembled as a separate unit which plugs into the main chassis via the cable connector P132 (Fig. 5). Components included within the dotted line of Figure 5 are mounted on a printed circuit board.

3.2 Voltage Regulators

As stated in the previous section +5 V, +15 V and −15 V regulated supplies are required. Conventional series type regulators (Fig. 6) provide these outputs which have been designated V_{CC}, V_{AA} and V_{BB} respectively.

Each supply circuit incorporates an integrated circuit regulating device (Q002, Q008 and Q009) with an external series transistor (Q003, Q007 and Q010) to effectively carry the load current. Potentiometer R003 allows the V_{CC} output to be adjusted, and potentiometer R026 allows the V_{AA} and V_{BB} outputs, which vary in unison, to be adjusted. (The internal reference for the negative regulating device Q009 is not utilized; V_{AA}, trimmed slightly via R024 for balance of the supplies, effectively constitutes the reference.)

Short circuit current limiting is provided for each output. In the circuit of Figure 6 these limits are 5·3 A for the V_{CC} supply and 125 mA in each case for the V_{AA} and V_{BB} supplies.

An overvoltage trip circuit incorporating Q004, Q005, Q006, K001 and associated components causes the V_{CC} output to be switched off if the voltage rises above a limit which could cause failures to occur in the many digital integrated circuits powered from this supply. Operating details for the trip circuit will be considered later in this section. For normal operation the K001 relay is de-energized (as shown in Fig. 6) and the V_{CC} circuit operates as a conventional regulator.

The following table indicates the current required from each supply for the circuits detailed in this report.

Supply	Nominal voltage	Current demand	
		Serial system	Parallel system
V_{CC}	+5 V	1·52 A	1·43 A
V_{AA}	+15 V	44 mA	44 mA
V_{BB}	−15 V	18 mA	18 mA

Since the hardware has been designed for future circuit expansion the power supply has been designed with considerable reserve of power. The capabilities of each supply will now be considered in detail. Performance figures quoted below were obtained using the 240 V mains input tapping (230 V and 250 V tappings also provided) on transformer L02 (Fig. 5).

The line regulation of the V_{CC} supply (for the V_{AA} and V_{BB} supplies each loaded at 100 mA) is summarized in the table on page 7. At 240 V line input, the V_{CC} output remains constant within 0·01 V from no load to 3·5 A load.

The line regulation of the V_{AA} and V_{BB} supplies (for the V_{CC} supply loaded at 4 A) is summarized in the table on page 7. At 240 V line input the V_{AA} and V_{BB} outputs each change by less than 0·01 V from no load to 100 mA load.

The overvoltage trip circuit used in conjunction with the V_{CC} supply is self-latching. Restoration of the V_{CC} supply to normal after the overvoltage circuit has tripped can only be achieved by momentarily switching off power to the interface via the front panel power switch.

Potentiometer R009 allows adjustment of the trip level, which has been set initially to 5·20 V. Such a setting ensures adequate input protection for series SN7400N TTL (transistor–transistor–logic) integrated circuits used extensively in the interface circuits.

The difference amplifier comprising Q004 and Q005 compares a proportion (adjustable via R009) of the reference voltage developed across CR002 with the V_{CC} output. CR002 provides a stable reference voltage (7·5 V nominal) which is independent of the reference within Q001. Under normal conditions Q004 is on while Q005 is off. R014 and C010 filter out any high frequency components (from the V_{CC} output) which would otherwise be coupled to the base of Q005.

If the V_{CC} output rises above 5·20 V for any reason both Q005 and Q006 will switch on. When Q006 switches on, the gate input voltage to the SCR (silicon controlled rectifier) CR004 will rise from near 0 V to about 2 V and the SCR will switch on. "Crow-bar" type operation will ensue for which heavy current will flow from the V_{CC} output via R017, CR003 and the anode of the SCR CR004. Capacitor C011 prevents the SCR from triggering on transient voltage "spikes" which could otherwise be coupled to the gate terminal.

When the SCR switches on, current will flow via the V_C input through the K001 relay coil (40 Ω resistance) to common via the SCR. Diode CR005 will prevent current from flowing through the relay coil until the SCR has switched on. The relay has a nominal 6 V coil which may initially have greater than 10 V developed across it. When the relay switches on, one set of contacts short the SCR and connect resistor R018 in series with the coil. The value of R018 is low enough to ensure that adequate current will flow through the coil to maintain the contacts in the "relay operated" state but is sufficiently high to ensure that the coil will not be over-heated if the overvoltage circuit is maintained in the tripped state for long periods. When the relay is operated, a further two sets of the contacts (connected in parallel) interrupt the current flow to the V_{CC} regulating circuit and connect R019 (which draws 0·5 A nominal) across the storage capacitor C02 in the AC to DC converter (Fig. 5). The remaining fourth set of contacts is taken to printed circuit edge connector pins. The corresponding contacts on the mating socket J120 may be utilized to actuate some external indicator if required.

Initially the trip circuit had a tendency to operate when load current was switched at the V_{CC} output (using a "simulated" load rather than the normal interface load). The addition of the bleed resistor R005, connected permanently across the V_{CC} output, together with the choice of suitable values for C010 and C011, completely eliminated the tendency of the trip circuit to operate when load current is switched.

Line regulation of V_{CC} supply									
Mains input voltage relative to 240 V	−10%	−7·5%	−5%	−2·5%	0%	+2·5%	+5%	+7·5%	+10%
V_{CC} for 3 A load	4·49 V	4·94 V	4·98 V	5·00 V	5·01 V	5·01 V	5·02 V	5·03 V	5·03 V
V_{CC} for 3·5 A load	4·07 V	4·44 V	4·69 V	4·96 V	5·01 V	5·01 V	5·02 V	5·03 V	5·03 V
V_{CC} for 4 A load	3·56 V	3·91 V	4·18 V	4·58 V	4·79 V	4·97 V	5·02 V	5·02 V	5·03 V

Line regulation of V_{AA} and V_{BB} supplies									
Mains input voltage Relative to 240 V	−10%	−7·5%	−5%	−2·5%	0%	+2·5%	+5%	+7·5%	+10%
V_{AA} for 50 mA load	+15·01 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V
V_{AA} for 100 mA load	+13·99 V	+14·33 V	+14·81 V	+14·96 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V	+15·02 V
V_{BB} for 50 mA load	−15·06 V	−15·06 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V
V_{BB} for 100 mA load	−14·03 V	−14·37 V	−14·85 V	−15·01 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V	−15·07 V

To prevent the trip circuit from operating when the front panel power switch S1 is switched on, the voltage at the base of Q004 must rise faster than the V_{CC} output. With the circuit time constants used such operation is assured.

The tendency of the trip to operate when mains power is interrupted or switched off has not been eliminated entirely. Under such circumstances the trip circuit may remain operated if mains power is quickly restored. The addition of R019 in shunt across C02 (Figs 5 and 6) makes it virtually impossible to manually switch power off and then back on "immediately" afterwards while the relay contacts are still closed.

3.3 Output Buffers

All outputs from the digital interface are buffered before being taken to the output connectors. To this end a general purpose output buffer printed circuit board (Fig. 7 and Appendix 3) has been included.

As the mating output cables are of relatively short length the type SN7404N hex inverter is considered to be a suitable output device. Output series connected resistors R101 to R156 provide some measure of output line matching and reduce currents in the event of output short circuits. Each input to the output buffer board is buffered and taken simultaneously to two output terminals. These outputs are coupled respectively to output connectors on the front and the rear panels.

Outputs to the tape machine may be taken via J102 (Appendix 4) on the front panel or J112 on the rear panel; outputs to the digital computer may be taken via J103 on the front panel or J113 on the rear panel.

Inputs to the output buffers may be transferred to the outputs without inversion if links A (Fig. 7) are inserted, or inverted if links B are inserted instead. The present link connections together with output connection details are given in Appendix 3.

Up to 28 outputs may be buffered. At present all these outputs are not utilized. However, all of the buffer outputs have been connected to the front and the rear connectors respectively. If future expansion indicates the need for any more outputs these may be simply connected to the appropriate buffer inputs and suitable links inserted on the output buffer board.

3.4 Input Clock Signal Generator

As indicated in Section 2 input signals to the digital interface are in NRZ code. For the serial system a two-line output (comprising an NRZM and an NRZS signal) as illustrated in Figure 1 is coupled from the digital tape reproducing amplifier outputs to the input connector J101 (Appendix 4) on the front panel of the interface or to J111 on the rear panel. For the parallel system a seven-line output (all signals being in NRZM code with the seventh carrying odd parity information) is coupled from the tape reproducing amplifiers to either of the input connectors (J101 or J111) used also for the serial system.

Data in NRZ code require a suitable clock signal in order to be read.

For the serial system a transition on the NRZM or the NRZS signal line signifies the presence of a "1" or a "0" respectively. The input clock signal generator detects a transition on either of these inputs (a transition on both these lines simultaneously should never occur) and generates an output clock signal required subsequently for reading the data.

For the parallel system, with the odd parity signal on the seventh line, a transition on at least one of the seven input lines occurs for each encoded byte of data.

The same input clock signal generator (Fig. 8) is used for both serial and parallel systems.

Inputs to the clock signal generator have been designated NRZ1 to NRZ7 (Fig. 8). In the case of the serial system the NRZM signal is taken to the NRZ1 input, the NRZS signal is taken to the NRZ2 input, and the other inputs are left open circuit.

Input circuits, to which the NRZ1 to NRZ7 inputs are coupled, are identical in each case so the operation will be examined with reference to the NRZ1 circuit only. Resistor R208 establishes a guaranteed "1" state for open circuit inputs. Inverter Q201A improves input signal rise time which may have been degraded somewhat in passing from the digital reproducing amplifier to the digital interface via coaxial cable, and then via the high frequency input noise

filter comprising R201 and C201 to the input of that inverter. The inputs to NOR gate Q204D are normally low but when a transition takes place on the NRZ1 input a positive pulse will be capacitively coupled to one of the NOR gate inputs thus switching the output of that gate low. Pulse duration is defined by the coupling networks comprising C208 and R215 or C209 and R216. In this case the duration has been set to about 4 microsecond. The output of NOR gate Q204D constitutes the A_1 clock signal (Fig. 8), and similarly for the A_2 to A_7 clock signals. Generation of the logical AND function $A_1A_2A_3A_4A_5A_6A_7$ (designated by A) is provided by Q206 and Q202D. For the serial system $A_2 = A_3 = A_4 = A_5 = A_6 = A_7 = 1$ and hence in that case $A = A_1A_2$.

For the parallel system it is possible to obtain more than one "A" output pulse per byte of data (particularly when the data are reproduced at low tape speeds for which time differences between transitions on the various input lines may exceed the "4 microsecond" duration). Moreover it is possible that the "A" pulse duration may exceed the "4 microsecond" by a time interval approximately equal to that between the earliest and the latest input pulse transition for the particular byte of data in question. Deskewing of the parallel data is performed with the aid of the electronic flywheel discussed in the following section.

Inverters Q202C, Q201C and Q201D are spare and are taken to the edge connector for future use if required.

3.5 Electronic Flywheel

As indicated in Section 2 suitable "gaps" (time intervals, longer than a normal bit repetition period, during which no digital information is encoded) are used to separate words and records (or frames) when the serial system of digital encoding is used. An essential requirement[3] of the digital interface is that it read digital data reproduced by the analogue reproducing machine at any tape speed in the range 4·76 cm/s ($1\frac{7}{8}$ ips) to 152·4 cm/s (60 ips). Corresponding bit repetition rates over this tape speed range are 640 to 20,480 bits per second. Recognition of the gaps involves the use of analogue techniques since a gap is, in effect, a time interval during which no transition occurs on either the NRZ1 or the NRZ2 inputs.

When the parallel system of encoding (refer Section 2) is used gaps are not used. Encoded digital information indicates the start of each word and of each record. Hence digital techniques can be used for separating the reproduced data into words and records.

To allow the gaps in the serial data to be detected at all the tape reproducing speeds a special "electronic flywheel" circuit has been developed. Additional features included in the electronic flywheel make it ideal for deskewing the data encoded in seven-channel parallel form. Further the flywheel enables increased noise immunity to be realized when data encoded in either serial or parallel form are read.

A block schema of the electronic flywheel is drawn in Figure 9 and complete circuit details are given in Figure 10.

Whenever the sequence of incoming clock pulses is interrupted the electronic flywheel will insert pulses and the repetition period of the inserted pulses will be automatically adjusted close to that of the incoming clock pulses. If the incoming pulses are stopped the repetition period of the free oscillations will gradually increase.

Incoming clock pulses (entering via the "A" input) are coupled to the delay producing monostable multivibrator or "one shot" (subsequently referred to as "delay monostable" or as "monostable"). The monostable Q301 establishes a constant time interval during which the output of the fixed slope ramp generator (comprising Q303, Q304 and associated components) is reset to zero. It is essential that sufficient reset time be provided to allow the ramp capacitor C304 (or C305 as selected by the plug-in link device LK301) to discharge completely through Q303 during this time. Normally at the time of arrival of input clock pulses A, the levels at E and F (Figs. 9 and 10) are high ("one" state) and the delay monostable is triggered on the negative going transitions of the A pulses where an A pulse is indicated by a change from a high level to a low level for a time duration of about 4 microsecond (Section 3.4). The delay provided by the monostable has been set to 1·4 microsecond approximately which is short compared with the lowest bit repetition period of interest (48·8 microsecond at 152·4 cm/s tape reproducing speed).

When input pulses *A* are applied, the repetition period of the ramp voltage waveform will be adjusted to that of the pulses. The ramp output is taken to a peak-charging circuit which converts the ramp voltage peaks (proportional to input "clock" pulse repetition period) into a steady output signal (also proportional to input clock repetition period). The ramp output is attenuated and compared with the output of the charging circuit. When input clock pulses are applied, comparator 1 (Fig. 9) does not switch. However, if the input clock pulse train is interrupted, this comparator will switch and send back pulses which reset the ramp output to zero. Hence in the temporary absence of incoming clock pulses the ramp will free run with a repetition period somewhat longer than that of the input clock. Waveforms drawn in Figures 11*a* and 11*b* indicate the operation of the electronic flywheel for serial data encoded using frame synchronization types A and B (Section 2) respectively.

Negative going clock pulses *E* of relatively short duration are generated during EOW and EOR gaps (where some input clock pulses *A* are received during the "EOR gap" for frame synchronization type B) and are fed back to the delay monostable input. These pulses, like the *A* pulses, trigger the monostable on the negative going transitions. A deskewed clock signal *F* (to be considered later in this section) is fed back to the monostable to prevent the latter from being triggered until a certain proportion of a bit repetition period has elapsed since the arrival of the last *A* or *E* pulse.

The ramp generator (Fig. 10) utilizes a conventional bootstrap sweep arrangement, with emitter follower Q305 output to prevent loading of the ramp charging circuit. Ramp slope is determined approximately by the supply rail voltage (V_{AA}) divided by the product of R305 and C304 (or C305). Hence a slope of approximately 8·3 V per millisecond is provided. In the following table the approximate peak ramp voltage excursion is given as a function of the bit repetition period (interval between input clock pulses) for various tape reproducing speeds.

Tape speed		Bit repetition period (microsecond)	Peak ramp output (V)
cm/s	ips		
152·4	60	48·8	0·40
76·2	30	97·6	0·81
38·1	15	195·3	1·62
19·0	$7\frac{1}{2}$	390·6	3·25
9·53	$3\frac{3}{4}$	781·3	6·50
4·76	$1\frac{7}{8}$	1562·5	13·00

The ramp output is reset to zero by the output NAND gate Q302A which inverts and provides buffering for the monostable output *D*. Note that *D* constitutes the output clock and includes clock pulses corresponding to both the input clock *A* and the inserted clock *E*.

The peak charging circuit comprising Q306 and associated components generates a steady voltage (across C308) proportional to the average repetition period of the *D* output clock.

Potentiometer R316 attenuates the ramp circuit output which is then coupled to one input of the voltage comparator Q307. The output of the peak detector circuit is coupled to the other input of the comparator. If the input clock *A* is interrupted the output of the peak detector circuit will tend to remain unchanged. The ramp voltage will continue to rise until coincidence is reached at the comparator input. At this time a reset signal will be sent back to the ramp generator via the monostable Q301. Such reset signals constitute the inserted clock (Figs 11*a* and 11*b*). Adjustment of R316 enables the ratio of the inserted clock repetition period to the input clock repetition period to be varied. These periods may be made very close if desired. In the present application the inserted clock repetition period is set manually 15% higher than the incoming clock repetition period. If R316 is adjusted so that the ramp slope is too high, triggering of the voltage comparator will occur between input clock pulses and the circuit will tend to

oscillate at high frequency. Increased comparator switching speed is provided by virtue of positive feedback via C311.

Some additional components not already mentioned have been added to the flywheel circuit.

Zener diode CR301 prevents failure of NAND gate Q302A which could otherwise receive excess voltage at the time power is first applied (particularly if card is plugged into a "live" socket such that the −15 V supply is applied before the +15 V supply). Diode CR303 used in the peak detector circuit provides some cancellation of the forward base-emitter voltage drop of Q306, and thus tends to equalize the peak ramp output at the emitter of Q305 with the peak output of Q306. Zener diodes CR304 and CR305 limit the output voltage swing for each comparator and ensure that the outputs are compatible with the TTL logic circuits they drive.

Resistors R314, R315 and R317 allow an adjustable DC offset to be added to the comparator ramp input. At high input clock frequencies (20·48 kHz maximum in this case) DC imbalances between the ramp output and the output of the peak charging circuit become very significant as the peak ramp voltage is low. Normally the system is first adjusted by setting R316 to give the appropriate ratio of the incoming clock repetition period to the inserted clock repetition period at 640 Hz input clock frequency and then by adjusting R314 to give the same ratio at 20·48 kHz input clock frequency.

High frequency bypass capacitor C303 has been added to prevent ramp circuit instability.

Capacitive coupling of the inserted clock pulses is provided by C315. Such coupling is required to ensure that the inserted clock input *E* of the delay monostable Q301 cannot remain permanently in the low state. If direct coupling were used instead, a stable condition could exist for which the *E* input is low (ramp charged to maximum value) and the input clock *A* is inhibited from initiating pulses in the monostable.

As mentioned earlier the electronic flywheel is also required to generate a "deskewed" clock defined as a clock signal (applied to a number of parallel digital data lines) which enables all data lines corresponding to each byte of data to be interrogated when all data lines have had time to change and at a time prior to the arrival of the next byte of data.

For data encoded in serial form only one level change will be generated per data bit (excluding parity errors). Hence a deskewed clock pulse which occurs a fixed time duration after each input clock pulse would be sufficient in that case. The time duration would need to be somewhat less than the minimum repetition period of interest (48·8 microsecond) to enable data to be reproduced at all speeds without switching. However, as will be indicated shortly, the generation of a deskewed clock which is delayed with respect to the input clock by a time interval proportional to the input clock repetition period, increases immunity to noise.

For data encoded in parallel form however, the input clock pulse generator (Section 3.4) may produce a number of input clock pulses per byte of data. Dynamic skew characteristics of the reproduced data will define the time difference between the various input clock pulses generated by each byte of data. To read such data over the full range of tape reproducing speeds, a clock delayed by a time inversely proportional to tape speed is required since time differences arising due to dynamic skew will be very nearly inversely proportional to tape speed.

The use of a second comparator as indicated in Figures 9 and 10 enables the required deskewed clock to be generated. In this instance the ramp output is coupled to one side of the comparator Q308 via potentiometer R322. A specified fraction of the charging circuit output voltage as set by R312 and R313 is coupled to the other input of the comparator. R319 allows for DC adjustment similar to that required for the inserted clock comparator Q307. Increased switching speed of the comparator is achieved by positive feedback via C314.

In the present application comparator Q308 has been set to switch nominally 40% of an input clock pulse repetition period after the arrival of the previous input or inserted clock pulse.

By coupling the deskewed clock output *F* (Figs. 9 and 10) back into the delay monostable Q301, only one clock pulse per data bit for the serial system, or per data byte for the parallel system, is guaranteed. Whenever the *F* input is low the monostable will not respond to pulses either on the *A* input (input clock) or the *E* input (inserted clock). For the first nominal 40% of the input repetition period the *F* input will be low. Hence a certain level of immunity to noise is achieved. It may be assumed that the *G* input to the NAND gate Q302C, providing coupling between comparator Q307 and the delay monostable, is high at the time of arrival of any input clock pulses.

At the time of arrival of the first input clock pulse after an EOW gap (serial system) the deskewed clock is always high and hence the first input clock pulse will trigger the delay monostable.

If the deskewed clock were generated normally throughout an EOR gap (during which a a large number of inserted clock pulses are generated) when frame synchronization type A (Section 2) is used, there would be no guarantee that the deskewed clock output *F* would be high at the time of arrival of the first input clock pulse after the EOR gap, and hence the output clock *D* may not immediately synchronize with the input clock as required. To prevent such an occurrence an inhibit signal *G*, which switches from a normally high state to a low state after 12 successive inserted clock pulses have been counted, and remains in that state until the arrival of the next input clock pulse, is provided by the control signal generator described in Section 3.6. An alternative signal *J* (Section 3.6) which inhibits during EOW gaps as well may be used in lieu of the *G* signal.

The filter circuit comprising R328 and C316 delays the application of inhibit signals for the delay monostable long enough to ensure that the first input clock pulse *A*, after an EOR gap, is not inhibited by the deskewed clock signal *F*.

One of the most important requirements of the electronic flywheel is that only one stable condition (corresponding to one output clock pulse per input clock pulse except during gaps) be possible when an input clock is applied. Certain other stable conditions are possible if some of the operating characteristics are incorrectly adjusted. A characteristic of particular importance is the ratio of the free-running period to the input clock period (adjusted via R316). If the free-running period is set too close to the input clock period, "double" frequency operation may occur in which an inserted clock pulse is generated between each successive pair of input clock pulses. Hence in that case two ramp peaks would be generated between each pair of input clock pulses and the output of the charging circuit would remain low. For the circuit of Figure 10, adjusted as described earlier, double frequency operation does not occur. Another stable operating mode is possible in which the output of the peak charging circuit charges to a voltage higher than that for normal operation. Under these conditions output clock pulses would not be generated for each input clock pulse. This mode of operation is very likely if the deskewed clock is delayed later than the mid-time between input clock pulses. It is also favoured by data containing gaps which represent a fairly large proportion of the total time especially if relatively long time constants are used in the peak charging circuit. In the application under discussion it has been found that for records composed of more than three data words between EOR gaps this latter operating mode does not arise. It is to be noted that in all cases correct operation represents at least one of the possible operating modes.

Because the voltage drops across the capacitors in the peak charging circuit can only change relatively slowly, the flywheel will not respond instantaneously to the application of an input clock but will take some time to change from quiescent mode (no input pulses) to synchronized operation. However, since analogue tape transports will also not respond instantaneously at switch-on, the small additional delays were not considered to be significant. It has been found that the time to change from quiescent mode to synchronized operation at 20·48 kHz input clock frequency is less than one second. Similarly the time to change from synchronized operation at 20·48 kHz to synchronized operation at 640 Hz is also less than one second. If instantaneous operation were required it would be necessary to initially break the flywheel circuit at Point X (Fig. 10) and apply a suitable DC potential to the comparator side.

By using a different value for the ramp capacitor, and hence changing the ramp slope, operation over a different input clock frequency range can be achieved. In the interests of circuit versatility changing the ramp capacitor is made convenient with the use of the plug-in linking device LK301. Selection of C304, C305 or an external capacitor (mounted within the link package) is possible.

Adjustment of the inserted clock free-running period (nominally 15% higher than the input clock repetition period) and of the delay of the deskewed clock (nominally 40% of an input clock repetition period) is performed via the various potentiometers used in the flywheel circuit, with ramp capacitor C304 selected, to provide synchronized operation over the input clock frequency range of 640 Hz to 20,480 Hz. Without readjustment of any of the potentiometers in the flywheel circuit synchronized operation over the input clock frequency range 1808 Hz to 40,960 Hz is made possible simply by selecting ramp capacitor C305 (in lieu of C304) via a

new link package LK301. It is possible to select the latter extended frequency range in the associated airborne data acquisition equipment.[2]

The performance of the flywheel over the full frequency range of interest has been checked and relevant details are given in the next table for which the following are defined—

(i) P_1 is the proportion of a normal input clock repetition period by which the second inserted pulse E in a word gap lags the instant the pulse would be received if the input clock continued regularly throughout the gap. As mentioned earlier the nominal value of the inserted pulse repetition period is 15% higher than the input clock repetition period, hence the nominal value of P_1 is 0·30 (equal to $2 \times 0{\cdot}15$).

(ii) P_2 is the proportion of a normal input clock repetition period by which the deskewed clock F (the positive transition) is delayed with respect to the input clock pulse. Since the nominal delay for the deskewed clock is 40% of an input clock repetition period the nominal value of P_2 is 0·40.

(iii) P_3 is the proportion of a normal input clock repetition period by which the deskewed clock pulse (positive transition), generated in relation to the second inserted clock pulse in a word gap, precedes the first input clock pulse in the following word. It follows that $P_3 = 1 - (P_1 + P_2)$ and hence has a nominal value of 0·30.

Values given in the following table were obtained for input data containing word gaps but no frame gaps (as would be produced for data encoded using frame synchronization type A or type B).

Input clock A repetition frequency (Hz)	Ramp capacitor = C304 (18K) Flywheel aligned at 640 & 20,480 Hz			Ramp capacitor = C305 (10K) No realignment of flywheel		
	P_1	P_2	P_3	P_1	P_2	P_3
500	0·22	0·36	0·42	—	—	—
640	0·30	0·38	0·32	—	—	—
800	0·31	0·40	0·29	0·12	0·30	0·58
1,000	0·32	0·40	0·28	0·22	0·34	0·44
1,280	0·33	0·40	0·27	0·35	0·37	0·28
2,000	0·32	0·40	0·28	0·39	0·39	0·22
4,000	0·29	0·40	0·31	0·37	0·40	0·23
5,120	0·27	0·39	0·34	0·35	0·40	0·25
7,000	0·25	0·39	0·36	0·32	0·40	0·28
9,000	0·24	0·39	0·37	0·31	0·40	0·29
10,240	0·24	0·39	0·37	0·30	0·40	0·30
15,000	0·27	0·41	0·32	0·28	0·41	0·31
20,480	0·31	0·42	0·27	0·27	0·42	0·31
30,000	0·45	0·45	0·10	0·27	0·44	0·29
40,960	—	—	—	0·31	0·47	0·22
50,000	—	—	—	0·36	0·48	0·16

When frame gaps are included in the input data signal the performance will be somewhat modified. Storage capacitor C308 will charge to a higher potential than it would if only word gaps were included. Some increase in the repetition period of the inserted clock will result, and the effect will be most pronounced in the word gap following the first word in a new data frame. In the following table the value of P_1 (defined above), for the word gap following the first data word after a frame synchronizing word, is given as a function of the number of words (other than the frame synchronizing word) in a data frame. As frame synchronization type B causes

less departure from "normal" (i.e. as for the previous table) than is the case for frame synchronization type A, measurements for the following table have been obtained for the latter form of frame synchronization only.

Values of P_1								
Input clock A repetition frequency (Hz)	Numbers of words per frame							
	1	2	3	4	5	7	10	50
640	0·41	0·41	0·40	0·39	0·39	0·39	0·39	0·38
1,280	0·72	0·52	0·50	0·47	0·46	0·45	0·45	0·45
2,000	0·79	0·64	0·49	0·46	0·44	0·43	0·42	0·42
2,560	0·80	0·54	0·47	0·43	0·42	0·41	0·40	0·39
5,120	0·68	0·47	0·41	0·38	0·35	0·33	0·32	0·31
10,240	0·58	0·42	0·35	0·33	0·31	0·30	0·29	0·28
20,480	0·70	0·50	0·43	0·40	0·38	0·36	0·34	0·32

The increase in the P_1 values relative to the earlier table is evident in the above table. Operation of the flywheel for frames containing less than three data words is unsatisfactory. For one-word frames the flywheel can lock to a sub-multiple of the input clock frequency and for two-word frames there is a tendency for the first information bit in the second word to be locked out.

Some of the salient features of the electronic flywheel are summarized in the following paragraph.

The flywheel circuit of Figure 10 is required in both the serial and the parallel systems of recording. For the serial system, inserted clock pulses generated during the EOW and EOR gaps may be counted (Section 3.6) and used to synchronize the data. In addition clock pulses are inserted if input pulses are missed due to tape dropouts or for other causes. For the parallel system gaps are not introduced but clock pulses are inserted if input pulses are missed as in the serial system. A deskewed clock generated by the flywheel enables data recorded either serially or in parallel to be read at suitable times. Further the deskewed clock is used to provide a measure of immunity to noise in association with the incoming clock. All the above functions are automatically performed without the need for switching any components in the flywheel circuit over the required input clock frequency range of 640 Hz to 20·48 kHz. One particular advantage of the flywheel circuit used is that ramp linearity is not of prime importance since the peak charging circuit follows any non-linearity.

3.6 Control Signal Generator

The control signal generator (indicated in the block schema of Figure 4) is required to generate:

(i) an inhibit signal G (at the end of each record or frame) for use with the electronic flywheel in the case of data encoded serially and employing frame synchronization type A;

(ii) a regular output clock signal which is coupled, after suitable buffering (Section 3.3) to external connectors J102 and J112 (Appendix 4) for subsequent use in the reading of multiplexed FM (frequency modulated) analogue data;

(iii) appropriate inhibit and clock signals for the serial to parallel converter (Section 3.7) and associated parity check circuits;

(iv) word read command and frame synchronizing signals for use with a digital computer;

(v) clock signals to enable the digital data to be read into data stores used in conjunction with displays (Sections 3.8 and 3.9);

(vi) a clock signal for use with the tape machine preset stop signal generator (Section 3.8).

The block schema of Figure 12 indicates in general terms the operating principle of the control signal generators for both the serial and the parallel systems. For simplicity not all the control functions have been indicated. For every 20 flywheel output clock pulses received by the bit counter in the serial system an output pulse is generated (each word has 20 bit durations associated with it), and for every four flywheel output clock pulses received by the byte counter in the parallel system an output pulse is generated (each word has four byte durations associated with it). Similarly the word counter counts the bit (or byte) counter output pulses (one for each word) but in this case the maximum count registered will be dependent on the number of words recorded per frame.

Synchronization of the bit (or byte) and the word counters is provided by the word and frame synchronizing signals generator. For the serial system counting of inserted flywheel clock pulses, which are received in the absence of flywheel input clock pulses, is employed in the synchronizing signals generator, whereas for the parallel system the recorded information is examined by the synchronizing signals generator.

The bit (or byte) counter outputs and the word counter outputs are decoded respectively by the serial to parallel converter control signal generator and the display control signal generator.

As the requirements of the control signal generators used respectively for the serial and parallel systems of digital recording are different the generators will now be considered separately.

Complete circuit details of the control signal generator for the serial system are drawn in Figure 13.

The timing relationships of some of the signals relevant to the control signal generator are indicated in Figures 14, 15 and 16. Figure 14 applies for all words except the frame synchronizing word W_0 (defined later in this section), whereas Figures 15 and 16 apply for the frame synchronizing word W_0 when frame synchronization type A and type B (Section 2) respectively are used.

Generation of appropriate control signals is made convenient by the use of a bit counter and a word counter. For each word (except the frame synchronizing word) 20 flywheel output clock pulses D are generated where two of these correspond to flywheel inserted clock pulses generated during the EOW (end-of-word) gap. To provide a divide-by-20 circuit the bit counter uses count-by-two flip-flop Q406B (Fig. 13) followed by decade counter Q408. Records (or frames) containing up to 100 words are accommodated using two decade counters Q412 and Q413 in the word counter.

The input clock signal H to the bit counter (i.e. at pin 6 of Q406B) is $(DG)'$ in logic notation (where the "dash" signifies an inversion). G remains high throughout all words except W_0. Switching of the bit counter occurs in synchronism therefore, with the positive going edges of the flywheel output clock D pulses. (The duration of the D pulses is 1·4 microsecond approximately as indicated in Section 3.5 and the negative going edges of these pulses occur in synchronism with the negative edges of the flywheel input clock A or the flywheel inserted clock E.)

The bit counter outputs switch in a straight binary sequence up to 19 as indicated in the table below. For convenience the outputs have been designated D_0, D_1, D_2, D_3 and D_4 (Fig. 13).

Each word may be subdivided into time intervals (bit periods) B_0 to B_{19} associated with each count state. In a logical context B_r is a quantity which takes on a high (logical "one") value for the period during which the bit counter registers the count state corresponding to B_r in the following table.

Bit period	State of bit counter				
	D_4	D_3	D_2	D_1	D_0
B_0	0	0	0	0	0
B_1	0	0	0	0	1
B_2	0	0	0	1	0
B_3	0	0	0	1	1
B_4	0	0	1	0	0
B_5	0	0	1	0	1
B_6	0	0	1	1	0
B_7	0	0	1	1	1
B_8	0	1	0	0	0
B_9	0	1	0	0	1
B_{10}	0	1	0	1	0
B_{11}	0	1	0	1	1
B_{12}	0	1	1	0	0
B_{13}	0	1	1	0	1
B_{14}	0	1	1	1	0
B_{15}	0	1	1	1	1
B_{16}	1	0	0	0	0
B_{17}	1	0	0	0	1
B_{18}	1	0	0	1	0
B_{19}	1	0	0	1	1

Words will be represented using a similar notation W_r (with similar logical meaning) to that used for bits. However, it is essential to distinguish between the recorded frame synchronizing word defined as W_0 in Figures 2 and 3 and the "word" which corresponds to the "00" state of the word counter. If n words (apart from the frame synchronizing word) are encoded then the word counter will initially switch to the "$n + 1$" state at the start of the recorded frame synchronizing word and only to the "00" state (defined as the W_0 state in this section) some time later (but prior to the start of W_1).

In the absence of reset signals the word counter will count up to 99. For records less than 99 words (apart from the frame synchronizing word) in length, resetting to the zero count state (associated with W_0) will occur during W_0. Hence the first information word in a record is W_1.

Reset signals are required to synchronize the bit and the word counters. To generate these, counting of the flywheel inserted clock pulses E is employed. The portion of the control signal generator relevant to the counting of flywheel-inserted clock pulses and the generation of appropriate control signals comprises Q401, Q406A, Q402, Q403, Q404 and associated components.

The count state of Q401 and Q406A indicates the number of E pulses received. Resetting of these circuits to zero count state occurs after four successive A pulses (counted by Q404) are received with no E pulses interposed. The outputs of Q401 and Q406A are coupled to the BCD to decimal decoder Q402 in the arrangement shown in Figure 13. The inputs to the decoder follow the logical sequence indicated in the following table.

Capacitive coupling to the "C" input of the decoder ensures that this input will switch high for a short time when the "B" output of the decimal counter Q401 switches high.

Number of E pulses received	Logical inputs to BCD to decimal decoder				Decimal equivalent of decoder input
	D	C*	B	A	
0	0	0	0	0	0
1	0	0	1	0	2
2	0	1	0	0	4
3	0	0	1	0	2
4	1	0	0	0	8
5	1	0	1	0	10
6	1	1	0	0	12
7	1	0	1	0	10
8	0	0	0	1	1
9	0	0	1	1	3
10	0	0	0	1	1
11	0	0	1	1	3
12	0	1	0	1	5

* Note the AC coupling to this decoder input means that the "1" state is momentary only.

At the end of each word two consecutive inserted clock pulses E are generated (Fig. 14) and hence a pulse will be generated on the decoded "4" output of the BCD to decimal decoder Q402 (as indicated in the previous table). This pulse sets the flip-flop comprising NAND gates Q403C and Q403D. Thus the $\bar{Q}$ output of Q403D switches low at the arrival of the second inserted clock pulse E during an EOW gap and remains low till the negative transition of the next A pulse.

The "D" output of the decade counter Q408 is inverted via Q415C to provide the U control signal output (Fig. 14) where

$$U = (B_{16} + B_{17} + B_{18} + B_{19})'.$$

The U signal output is taken to the analogue tape machine preset stop signal generator (Section 3.8), and is also significant in the generation of J and M control signals (Fig. 13).

Throughout all word durations except W_0 the Q output of Q403B will be low and hence the control signal J output (Fig. 14) of NOR gate Q409C approximates B_{19} (but the trailing edge of the J pulse arrives about 1·4 microsecond before the trailing edge of B_{19}) for all words except W_0.

Control signal J resets the bit counter comprising Q406B and Q408 to the B_{19} state. It is also used in conjunction with the serial to parallel converter (Section 3.7). In the absence of the J pulses the bit counter would switch (after initial synchronization) to the B_{19} state about 1·4 microsecond (the duration of a D pulse) after the arrival of the second E pulse. Thus the J reset signal causes the bit counter to advance "early" (Fig. 14).

Recognition of the frame synchronizing word W_0 is essential to allow generation of:

(i) a reset signal for the word counter comprising Q412 and Q413;

(ii) a reset signal (for the bit counter) which is generated on the J output control line during the W_0 word duration;

(iii) an inhibit signal G for use with the electronic flywheel;

(iv) a frame synchronizing signal for the digital computer (any particular word is identified by counting "Read Command" pulses I generated since the previous frame synchronizing word).

The circuit logic has been chosen such that the interface equipment will automatically read data encoded using either frame synchronization type A or type B (Figs. 2 and 3) without the

need for component change or switching. To realize this, the following algorithm which, as may be seen by examination of Figures 15 and 16, is satisfied by both systems of frame synchronization, has been used.

> "Control signal G will switch low if 12 flywheel inserted clock pulses E are received without four flywheel input clock pulses A being received between any consecutive pair of E pulses. Control signal G will switch back high at the time of arrival of the next A pulse following the twelfth E pulse."

As indicated in the previous table a negative going pulse will be generated on the "5" output of the BCD to decimal decoder Q402 at the arrival of the twelfth E pulse. At this time the G output will switch low.

The D output of the divide-by-five circuit Q404 switches low at the time of arrival of each E pulse but switches back high, and resets the E-pulse counter comprising Q401 and Q406A, if four A pulses are counted since the previous E pulse.

While the inhibit signal G (Figs. 15 and 16) is low the flywheel deskewed clock output F is held high. The inhibiting function satisfies an essential requirement when frame synchronization type A is used (otherwise one or more flywheel input clock pulses A may be "missed" at the start of W_1 due to the inhibiting effect of the deskewed clock output F while this output is low). When frame synchronization type B is used, the flywheel inhibit signal G (Fig. 16) is coupled to the flywheel but such coupling is not a requirement.

The G' signal (output of Q403B) resets the word counter (Q412 and Q413) to count state "00" whenever it switches high.

Control signal J (Figs. 14, 15 and 16), used in conjunction with the serial to parallel converter (Section 3.7) and in the resetting of the bit counter, also switches low during the W_0 period together with the G signal. For all word periods except during W_0, when frame synchronization type A is used, J is given by

$$J = (B_{19}D)'.$$

Signal J can be used as the flywheel inhibit signal in lieu of the G signal. When the J signal is used, any inhibiting effect of the flywheel deskewed clock F is nullified at both the start of a new frame (as for G) and at the start of each word (in contrast to G). A marginal improvement in the flywheel upper frequency limit results if the J signal is used in place of the G signal.

Control signal N (Figs. 15 and 16) which switches low once for each frame of data, forms the frame synchronizing signal for use with the digital computer (Section 3.11).

The read command signal I for use in conjunction with the digital computer (Section 3.11) is inhibited whenever control signal N is low. At other times the I signal switches low for the duration of B_{18}. Logically we may write

$$I = (B_{18}N)'.$$

Filter components R403 and C403 prevent the generation of additional very short duration pulses on the I output as a result of propagation delays in the bit counter and associated decoding logic devices. The read command signal I has a minimum duration of about 50 microsecond at the maximum data rate used.

Control signals I_n, I_{11} and I_{12} (Figs. 13 and 14), which allow the display of any selected data, time-of-day and fixed data, have been provided.

Front panel mounted decimal thumbwheel switches[7] S5A and S5B, in association with the BCD to decimal decoders Q410 and Q411, allow any word between 01 and 99 to be selected for display.

I_n (Fig. 14) is given by

$$I_n = B_{18}\, W_n,$$

where n is the number set on switches S5A and S5B.

All fixed and time-of-day data are encoded in the first word of the record (W_1). Control signals I_{11} and I_{12} may be written logically as

$$I_{11} = B_{18}\, W_1\, F',$$

$$I_{12} = B_{18}\, W_1\, F.$$

Positive going transactions of the deskewed clock F occur about 40% of an input clock repetition period (Section 3.5) after the leading edges of the output clock pulses D. Coupling components C404 and R404 (Fig. 13) cause the generation of a short-duration (approximately 300 nanosecond) negative going pulse (which will be designated as F_1) at the output of Q415A for every positive transition of the F output. The output M of NAND gate Q414A consists of a series of negative going short duration pulses (Figs. 14, 15 and 16) inhibited for the period associated with bit counter states B_{16}, B_{17}, B_{18} and B_{19}. Logically we may write

$$M = B_{16} + B_{17} + B_{18} + B_{19} + F_1.$$

M forms the clock signal used in conjunction with the serial to parallel converter.

Input control signal K (Fig. 13) and output control signal L are used in conjunction with the serial to parallel converter and are logically related as follows.

$$L = B_{18} + B_{19} + K + F_1.$$

The FM clock signal (Fig. 13) is usable only when frame synchronization type B is used. In that case the negative transitions of the FM clock signal (Figs. 14 and 16) will always occur in synchronism with "recorded" transitions (for which A pulses are generated). Frame synchronization type B allows the generation of a regular FM clock signal during the time interval associated with the frame synchronizing word (Fig. 16). The regular clock signal is taken externally to J103 and J113 (Appendix 4) for use in the demultiplexing of FM data. Repetition period of the FM clock signal is four bit periods.

Complete circuit details of the control signal generator for the parallel system are drawn in Figure 17. The timing relationship of some of the signals generated is shown in Figure 18.

As indicated in Section 2 the end of a word and the end of a record (or frame) are indicated by information recorded digitally on two tape tracks (tracks 5 and 6). Four bytes of data are recorded per word. The information is recorded on tracks 1 to 4 and odd lateral parity is recorded on track 7. The second of two consecutive recorded "ones" on track 5 indicates the presence of the last of the four bytes in each word and the fourth of four consecutive recorded "zeros" on track 6 indicates the presence of the last byte in the record.

Generation of appropriate control signals is made convenient by the use of byte and of word counters. For each word, four output clock pulses D (Section 3.5) are generated. A divide-by-four counter made up of flip-flops Q457A and Q457B (Fig. 17) is used as the byte counter. Records containing up to 100 words are accommodated using two decade counters Q463 and Q464 in the word counter.

Appropriate signals are generated to reset the byte and the word counters. Since synchronizing information is contained in the digital data recorded on tracks 5 and 6 it is essential that these data be first read. Digital outputs e_5 and e_6, which change state according to the recorded data on tracks 5 and 6, are derived from the serial to parallel converter (Section 3.7). Serial to parallel conversion of the data recorded in parallel is used to convert the four serial bytes into one 16-bit parallel word with an additional parity checkbit. Any changes in state of e_5 and e_6 will occur during times that the A_5 and A_6 outputs from the input clock signal generator (Fig. 8) are low.

Short-duration (300 nanosecond approximately) positive going pulses starting at the trailing edges of the D pulses are generated using AC coupling between OR gate Q451C (used for input signal buffering) and OR gate Q451D. These pulses are suitably gated via Q455B and Q455D (NAND gates). When e_5 is low, flip-flop Q454A receives negative going pulses on the "clear" input in time synchronism with the trailing edges of the D pulses. When e_6 is high, flip-flops Q454B, Q458B, and that comprising NAND gates Q460C and Q460D, receive similar "clear" pulses.

Short-duration (300 nanosecond approximately) positive pulses S starting at the positive going transitions of the deskewed clock F (Fig. 18) are generated using AC coupling between OR gate Q451A (used for input signal buffering) and OR gate Q451B. These pulses clock flip-flops Q454A and Q454B (J–K flip-flops with $J = K = 1$) when e_5 is high and e_6 low respectively. After two consecutive "ones" are read from the NRZ5 input (Fig. 8), the $\bar{Q}$ output of flip-flop Q454A will undergo a positive transition at the time the deskewed clock F goes high. This latter transition is AC coupled to NAND gate Q460A which is gated also by the S clock. Hence an output (negative going) pulse will be generated by Q460A in synchronism with S whenever two

consecutive "ones" are read from the NRZ5 input to the interface. This latter output checks that the byte counter is in the count-of-three state. When the byte counter receives the next clock pulse *D*, it reverts to the count-of-zero state which corresponds to the first byte in the word. Whenever four consecutive "zeros" are read from the NRZ6 input to the interface, the $\bar{Q}$ output of flip-flop Q458B will switch high in synchronism with the *S* clock. This latter output sets the output of Q460D low (with the aid of NAND gate Q460B and the flip-flop action of Q460C and Q460D) in time synchronism with the *S* clock. A reset pulse in time synchronism with the *D* output clock pulse is generated by NOR gate Q459B and resets the word counter (comprising Q463 and Q464) to the zero state when the *D* pulse following the last "zero" read from the NRZ6 input arrives. Hence the word counter will take on the count state 00 (defined as the W_0 state) for the first word (i.e. the word immediately following that containing the frame synchronizing information) in the record. This is to be compared with the control signal generator for the serial system for which the corresponding state would be W_1. In each case the first word in the record contains time-of-day and fixed (e.g. run number) information.

Output *N* (Figs. 17 and 18) constitutes the frame synchronizing signal required for the digital computer. It is generated during the time interval associated with the frame synchronizing word. Information read by the digital computer on the next read command pulse (defined below) received after the *N* signal switches high corresponds to that encoded in the frame synchronizing word.

For records less than 100 words in length the generation of word counter reset pulses is essential to maintain synchronism whereas the generation of byte counter reset pulses is not normally required to maintain synchronism. Usually the byte counter reset pulses merely check that the state of the byte counter is correct.

Suitable clock signals (Fig. 18) for use with the serial to parallel converter are generated using four NOR gates Q453 and four AND gates Q452 in conjunction with the byte counter outputs and the *S* signal. These clock pulses are short duration positive pulses in time synchronism with the *S* signal. X_1 occurs only in association with the first byte, X_2 occurs only in association with the second byte and so on. Other signals required by the serial to parallel converter are the *S* signal described earlier and a signal designated *U* which is normally low but which reverts to the high state for the duration of the first byte (i.e. for the time the byte counter is in the count-of-zero state).

A pulse starting at the trailing edge (negative going transition) of the X_4 pulse presets the *Q* output of flip-flop Q458A (i.e. switches to high state) which is cleared back to the low state in synchronism with the next *D* pulse. The $\bar{Q}$ output of flip-flop Q458A constitutes the read command signal *I* (Fig. 18) required for the digital computer. The read command signal *I* is generated for each word and has a minimum duration of about 145 microsecond (corresponding to the maximum data rate of 1024 words per second).

Data display requirements are identical to those for the serial system. Front panel mounted decimal thumbwheel switches[7] S5A and S5B, in association with BCD to decimal decoders Q461 and Q462 allow any word between 00 and 99 to be selected for display. A control signal I_n (Fig. 18) having the same time relationship as the *I* signal, except that it is only generated for the selected word, is made available for use with the selected data display (Section 3.9). Similarly control signals I_{11} and I_{12} (Fig. 18) are generated for use with the fixed data and time-of-day displays (Sections 3.8 and 3.9). Both are generated in association with word counter state W_0; I_{11} is generated in time synchronism with X_4 and I_{12} in time synchronism with *I*.

The word counter takes on the highest count state (W_{N-1} for records containing *N* words including the synchronizing word (Fig. 18)) when the synchronizing word (which also contains information data) is decoded.

3.7 Serial to Parallel Converter

Rearrangement of the digital data as received by the interface is desirable for ease of handling by the digital computer which will accept a 16-bit parallel input. For data recorded serially (Section 2) a 16-bit serial to a 16-bit parallel conversion is required whereas for data recorded in parallel a four-byte serial (four data bits per byte) to a 16-bit parallel conversion is required. In addition parity checkbits have to be generated for each word. As the requirements for the

serial to parallel converters used respectively for the serial and the parallel systems of data encoding are different the converters will be considered separately.

Complete circuit details of the serial to parallel converter for the serial system are drawn in Figure 19.

For ease of explanation b_0 to b_{17} are defined as the digital information encoded sequentially, starting at b_0, for each word. Note that b_{18} and b_{19} are not included because EOW gaps (two-bit durations) are used. The following table summarizes the format of the encoded data.

Bit period	B_{19}	B_0	B_1	B_2	$B_3 \ldots B_{14}$	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	B_0
Information encoded on NRZ1 input	—	b_0	b_1	b_2	$b_3 \ldots b_{14}$	b_{15}	0	g	—	—	b_0
Information encoded on NRZ2 input	—	b_0'	b_1'	b_2'	$b_3' \ldots b_{14}'$	b_{15}'	1	g'	—	—	b_0'

B_0 to B_{19} refer to time intervals associated with each count state of the bit counter (Section 3.6).

During B_{17} the encoded longitudinal parity character g is received such that

$$g = 1 \text{ if } \sum_{r=0}^{15} b_r \text{ is odd,}$$

$$g = 0 \text{ if } \sum_{r=0}^{15} b_r \text{ is even.}$$

During B_{16} a dummy zero character ($b_{16} = 0$) is encoded. The addition of the dummy character enables both odd lateral and even longitudinal parity conditions to be satisfied at B_{17}.

Temporary storage (for the time allocated per bit) of the digital data encoded on the NRZ1 input is provided by the bistable circuit comprising NAND gates Q506A and Q506B, and storage of that encoded on the NRZ2 input is provided by the bistable circuit comprising NAND gates Q506C and Q506D. Each time a "one" is read from the NRZ1 input, input A_1 (Fig. 19) will switch from its normally high state to the low state for approximately 4 microsecond (Sec. 3.4) and each time a "one" is read from the NRZ2 input A_2 will switch in a similar manner. The A_1 and A_2 inputs preset the respective Q outputs of the above-mentioned bistable circuits to the "one" state whenever these inputs switch to the low state (i.e. whenever "ones" are read).

The H input derived from the control signal generator (Section 3.6) consists of a series of positive pulses (of 1·4 microsecond duration approximately) in time synchronism with the flywheel output clock signal D. While the flywheel inhibit signal G is low (Figs. 15 and 16) the H output remains high (Section 3.6):

$$H = (DG)'.$$

Clear signals $(A_1H)'$ and $(A_2H)'$ are taken to the temporary storage bistable circuits mentioned above. Since the A_1 or A_2 pulses and the D pulses are nominally coincident (but more precisely the D pulses are slightly delayed with respect to the A_1 or A_2 pulses which effectively initiate them) clear pulses (low level) will be generated only when a "zero" is read (i.e. when a "one" is read on the "other" input). In Figure 20 oscilloscope traces indicate the time relationship between A_1, A_2, H and the clear signals for the temporary storage bistables. Changes in state of these bistables always occur in synchronism with the leading edge of the D (or H) clock.

Serial to parallel conversion of the digital data is performed using four 4-bit shift registers Q501 to Q504 connected as a 16-bit shift register. The output of the bistable comprising Q506A and Q506B is connected to the serial input of the Q501 shift register. Clocking of the shift register is performed by the M' signal where M is a signal (Figs. 14, 15 and 16) generated in the control

signal generator. M' is normally low but switches high for a short period (approximately 300 nanosecond) starting at the time the deskewed clock goes high. Shift register clock pulses are generated only in association with bits b_0 to b_{15}. Whenever a clock pulse is applied to the shift register the level on the serial input is transferred to the first output and all the other outputs shift one place to the "right". Hence on the application of the sixteenth clock pulse (transfer of data occurs on the negative transition of the clock) the 16-bit register will contain the data word with b_{15} being the last bit entered into the register (Fig. 19). Since the shift register does not receive another clock pulse until b_0 of the next word is read, the contents of the register will remain unchanged from B_{16} to B_{19} (refer to Section 3.6 for definition). The outputs of the shift register have been designated b_0 to b_{15} but it must be remembered that these outputs are a true representation of the digital data only over part of a word repetition period.

Whenever a clock pulse is applied to the shift register (i.e. for b_0 to b_{15}) the lateral parity of the information as encoded on the NRZ2 input, and as read by the bistable comprising Q506C and Q506D, is checked using the exclusive OR circuit Q507A and NAND gate Q505C. If the parity is even (two "ones" or two "zeros") a negative going preset pulse will be transferred to flip-flop Q505C. At the beginning of each word the Q output of flip-flop Q508A is cleared to the low state (i.e. on the positive excursions of the J control signal (Figs. 14, 15 and 16) which occur at the start of each word). Hence if one or more lateral parity errors are detected in a word the Q output of flip-flop Q508A designated as p_1, will switch to a high state which will be maintained until the start of the next word.

The longitudinal parity of the word as read from the data track is checked using flip-flop Q508B and associated components. At the beginning of each word the Q output of flip-flop Q508B is cleared to the low state. This latter flip-flop (J–K flip-flop with $J = K = 1$) toggles each time a clock pulse is applied. A signal L' is connected to the clock input where (Section 3.6):

$$L = B_{18} + B_{19} + K + F_1.$$

As indicated earlier F_1 represents a signal which is normally low but which switches high for a short time (300 nanosecond approximately) whenever the deskewed clock F (Figs. 14, 15 and 16) switches from the low to the high state. K is the Q output of the bistable comprising NAND gates Q506A and Q506B. As can be seen from the above equation the clock L' will remain high for the time interval associated with B_{18} and B_{19} and hence flip-flop Q508B will not change state in this time. Otherwise clock pulses will be generated for every "one" read from the NRZ1 input. If the parity is correct an even number of clock pulses will be generated and the Q output of flip-flop Q508B, designated as p_2, will be low after b_{17} has been read. Conversely if the even longitudinal parity condition is not satisfied output p_2 will be high after b_{17} has been read.

An overall parity check character p (where $p = p_1 + p_2$) is also generated. When an error is detected on either or both of the lateral and the longitudinal check circuits, p will switch to the high state.

The parallel output comprising the 16 data bits (b_0 to b_{15}) and one or two parity bits (p or (p_1 and p_2)) is taken to the data stores (Sections 3.8 and 3.9) associated with the data displays. Reading of the parallel output is performed within the time associated with B_{18} (see waveforms relating to I, I_n, I_{11} and I_{12} in Figure 14). During this time of reading, the data are correctly arranged in the output register and no data changes are possible.

Complete circuit details of the serial to parallel converter for the parallel system are drawn in Figure 21.

Each time a "one" is read from a particular input the associated data output (A_1 to A_7 (Fig. 8)) from the input clock signal generator will switch from a normally high state to a low state for approximately 4 microsecond thus setting the output of the associated temporary storage bistable (comprising NAND gate Q551A and Q551B for A_1 and so on) to the high state. Each time a flywheel output clock pulse D arrives it sets the $\bar{Q}$ outputs of each bistable to the high state. Hence in the absence of a pulse (i.e. when a zero is read) on any given PR (preset) input (Fig. 21) the corresponding Q output will be set to the low state. NAND gates Q554C and Q554D which are connected as inverters provide buffering for the D input which would otherwise be loaded excessively (taking into consideration loading elsewhere).

The Q outputs of the temporary storage bistables comprising Q551A to Q554B have been designated e_1 to e_7 (Fig. 21). Outputs e_5 and e_6 are returned to the control signal generator (Section 3.6 and Fig. 17) and are used for synchronizing the byte and the word counters. Outputs

e_1 to e_4 are connected to four separately clocked four-bit bistable latches Q557 to Q560. Whenever the clock signal for a four-bit latch switches to the high state the digital input data signal on $1D$ to $4D$ respectively (Fig. 21) is transferred to the corresponding output ($1Q$ to $4Q$) where it is retained after the clock switches back to the low state. Clock signals X_1 to X_4 (Section 3.6) are short-duration positive pulses starting in time synchronism with the positive transitions of the deskewed clock. X_1 is generated only in association with the first byte, X_2 is generated only in association with the second byte and so on. Hence between the time the X_4 clock pulse is applied and the time the X_1 clock pulse for the next word is applied, the parallel output b_0 to b_{15} from the four-bit latches holds digital information corresponding to the last word read.

Data output e_1 to e_7 are connected to the parity checker Q561 to enable lateral parity to be checked. If the parity is odd the output of the parity checker will be low (normal); if the parity is even the output will be high (indicating an error). Interrogation of the output of the parity checker is performed using the S control signal (where $S = X_1 + X_2 + X_3 + X_4$) in conjunction with NAND gate Q555A. If a parity error is detected in one or more bytes of data corresponding to a particular word then the Q output p_1 of the bistable comprising NAND gates Q555B and Q555C will be preset to the high state. At the beginning of each word (i.e. on the positive going transitions of U (Fig. 18)) p_1 is cleared to the low state. U is buffered via NAND gates Q556C and Q556B and AC coupled via NAND gate Q556A to the clear input of the bistable comprising NAND gates Q555B and Q555C so that the clear pulse is of relatively short duration (300 nanosecond approximately). Hence between the time the X_4 clock pulse is applied (to four-bit latch Q560) and the time the X_1 clock pulse for the next word is applied (to four-bit latch Q557) the parity output p_1 indicates whether any parity errors have been detected in the last word read.

The parallel output comprising 16 data bits (b_0 to b_{15}) and the parity bit p_1 is taken to the data stores (Sections 3.8 and 3.9) associated with the data displays. Reading of the parallel output is performed within the time associated with I (Fig. 18) which constitutes a read pulse for each word. Similarly a read pulse I_n (Fig. 18), having the same time relationship in the word repetition period as I, is generated for use with the selected data display (Section 3.9). I_{11} and I_{12} (where $I_{11} + I_{12} = I_1$, putting $n = 1$ in I_n (Fig. 18)) are generated for use with the fixed data and time-of-day displays (Sections 3.9 and 3.8 respectively).

The parity checking arrangement employed for both the serial and the parallel systems provides an indication of whether there is an error (or a likely error) in a word. In the case of the serial data for which lateral and longitudinal parity bits are recorded it would be possible to locate single errors in a word and correct for these. However, considerable increase in circuit complexity would result. Since an occasional error is of no consequence for the type of data encoding envisaged (provided that the word in error can be located and ignored) the generation of overall word errors is considered adequate. Such error information may be used by a digital computer which may be programmed to ignore any word for which an error is indicated or to suitably label any output data which use information contained in such a word.

3.8 Time-of-Day Store and Tape Machine Preset Stop Signal Generator

The word immediately following that containing the frame synchronizing information is used for encoding fixed data and time-of-day information. Four such words recorded in successive frames specify one complete reading of the above data. A two-bit identifier read from the b_0 and b_1 outputs of the serial to parallel converter (Figs. 19 and 21) identifies the particular information contained in each of the four words.

For the serial system of encoding, the fixed data and time-of-day information will be read when the word counter is in the "W_1" state (Section 3.6), whereas for the parallel system such data will be read when the word counter is in the "W_0" state (Section 3.6).

The fixed data includes:

(i) Run number composed of four decimal digits where each digit is encoded in 1–2–4–8 binary coded decimal (BCD).

(ii) Month-of-the-year (1 to 12) and day-of-the-month (1 to 31) information encoded in 1–2–4–8 BCD using a total of 11 bits (five for month-of-the-year and six for day-of-the-month).

Time-of-day is encoded as hours (0 to 23), minutes (0 to 59) and seconds (0 to 59) in 1–2–4–8 BCD code using a total of 20 bits (six for hours, seven for minutes and seven for seconds).

Details of the encoding configuration used for the fixed data and the time-of-day information are given in the table on page 25.

To facilitate identification of magnetic tape records and to assist in locating any specific regions of interest on a particular tape the fixed data and the time-of-day data are displayed (Section 3.10) using numeric indicators mounted on the front panel of the digital interface. Display of any word as selected by a front panel mounted thumbwheel switch is also provided using numeric indicators. The word so diplayed will be referred to as "selected data".

To provide appropriate displays it is essential that the data be read into suitable stores. Separate printed circuit boards, discussed in this and the following section (Section 3.9) respectively, are used for:

(i) The "time-of-day store" which stores time-of-day (hours, minutes and seconds) and day-of-month information (which strictly speaking, forms part of the "fixed data") as read from frame 0 and frame 1 according to the table on page 25.

(ii) The "selected data and the fixed data store" which stores the "selected data" detailed in Section 3.9 and all the fixed data (excluding that relating to the day-of-the-month) read from frames 2 and 3 according to the table on page 25.

A "preset-stop generator", which enables the analogue magnetic tape reproducing machine to be stopped when any predetermined time-of-day is read, is included on the same printed circuit board as the time-of-day store.

Complete circuit details of the time-of-day store and the preset-stop generator are drawn in Figure 22.

On the positive transition of the control signal I_{11} (Figs. 14, 18 and 22) digital data b_0 and b_1 are entered into the bistable latch store Q610 (Fig. 22) and are transferred to the $1Q$ and $2Q$ outputs. Using NOR gates Q606 these outputs are decoded to provide a high output successively on each gate (with low outputs on the other three) according to the value of the b_0 and b_1 inputs at the time I_{11} is high.

Normally the T output (Fig. 22) is high such that the I_{12} control signal (Figs. 14, 18 and 22) is effectively gated, as summarised in the following table, to the outputs (defined as Y_1 to Y_4 in Fig. 22) of NAND gates Q605.

b_0	b_1	Y_1	Y_2	Y_3	Y_4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

The control signal I_{12} is always delayed with respect to the I_{11} signal (Figs. 14 and 18).

NAND buffers Q607A and Q607B invert the Y_1 and Y_2 outputs and provide sufficient drive capability to satisfy the requirements of the store clocks (having logical values of $\overline{Y}_1$ and $\overline{Y}_2$).

Time-of-day in minutes and seconds (outputs m_1 to m_{14}) is entered into stores included in binary latches Q610 to Q613 at the time Y_1 switches low (see previous table and that on page 25). Time-of-day in hours (outputs m_{15} to m_{20}) and day-of-month (outputs m_{21} to m_{26}) are entered into stores comprising bistable latches Q607 to Q609 at the time Y_2 switches low.

The time-of-day information recorded on the magnetic tape effectively constitutes an identifier which may be used for specifying the location of any areas of interest on the tape. To

Frame	Serial to Parallel converter output notation	b_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8	b_9	b_{10}	b_{11}	b_{12}	b_{13}	b_{14}	b_{15}
0	Detail	← Two-bit → identifier		← Time of day — Minutes →							← Time of day — Seconds →						
	Store output designation			m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}	m_{11}	m_{12}	m_{13}	m_{14}
	Digital value	0	0	×	×	×	×	×	×	×	×	×	×	×	×	×	×
1	Detail	← Two-bit → identifier		← Time of day — Hours →						← Fixed data — Day of month →							
	Store output designation			m_{15}	m_{16}	m_{17}	m_{18}	m_{19}	m_{20}	m_{21}	m_{22}	m_{23}	m_{24}	m_{25}	m_{26}		
	Digital value	0	1	×	×	×	×	×	×	×	×	×	×	×	×	—	—
2	Detail	← Two-bit → identifier		← Fixed data — Month of year →							← Fixed data — Run number (first two digits) →						
	Store output designation			m_{27}	m_{28}	m_{29}	m_{30}	m_{31}	m_{32}	m_{33}	m_{34}	m_{35}	m_{36}	m_{37}	m_{38}	m_{39}	m_{40}
	Digital value	1	0	×	×	×	×	×	—	×	×	×	×	×	×	×	×
3	Detail	← Two-bit → identifier								← Fixed data — Run number (last two digits) →							
	Store output designation									m_{41}	m_{42}	m_{43}	m_{44}	m_{45}	m_{46}	m_{47}	m_{48}
	Digital value	1	1	—	—	—	—	—	—	×	×	×	×	×	×	×	×

"×" means information bit (may be "0" or "1").
"—" means spare bit (at present encoded as a "1").

enable the analogue tape reproducing machine to be stopped at any predetermined location, a preset stop signal generator comprising eight-input NAND gate Q602 (Fig. 22), and dual-input NAND gates Q601A to Q601D and Q604A, has been incorporated.

Presetting of the required stop point of the tape transport is achieved using a total of eight front panel mounted thumbwheel switches (Section 3.10) which allow time-of-day (in hours, minutes and seconds) and day-of-the-month to be set. When the time-of-day and day-of-the-month read from the recorded tape corresponds with the information set on the thumbwheel switches a gating signal T (Fig. 22) is generated. This gating signal may be transmitted to the tape transport via a Remote Control[8] which converts the gating signal to a form compatible with the tape machine stop signal requirements.

The thumbwheel switches are decoding types (Section 3.10) requiring complementary inputs (m_1 and $\bar{m}_1$ to m_{26} and $\bar{m}_{26}$) from the time-of-day store (Fig. 22). Normally the switch outputs Z_1 to Z_8 (Fig. 22) are low, but when coincidence between the number set on any given switch and the decimal equivalent of the applied input from the time-of-day store, is reached, the corresponding output will switch to the high state. When coincidence is simultaneously reached on all switches the output of the eight-input NAND gate Q602 will switch to the low state.

Details of the time-of-day store output connections to the tape machine preset stop switches and the switch output (Z_1 to Z_8) connections to the preset stop circuit of Figure 22 are given in the associated document.[7]

Since the store outputs may not all be set at precisely the same time, it is essential that an inhibit signal be applied so that the output of the eight-input NAND gate Q602 is not interrogated at times when the data in the store are being changed. Control signal U (Figures 13 and 14 for the serial system, Figures 17 and 18 for the parallel system) provides the required inhibit function when low. NAND gates Q601A (connected as an inverter) and Q601B produce the desired effect. A preset pulse (low state) is coupled to the bistable comprising NAND gates Q601C and Q601D only if $Z_1Z_2Z_3Z_4Z_5Z_6Z_7Z_8 = 1$ and $U = 1$. Once having been preset the output of Q601D will remain high. Provided the $S2$–W input (Fig. 22) is high (which will be so only if the Tape Machine Preset Stop function is switched "on" at the front panel) the preset stop output T will switch low and remain low when coincidence of the preset data and the decoded time-of-day data is reached.

Since at the time the interface is switched on the output of Q601D may be either high or low it is essential that the bistable be cleared (output of Q601D set low) before the tape is set in motion (or an attempt is made to do so since, if the output of Q601D is high, the machine will be stopped). Depressing the front panel mounted "START" pushbutton prior to setting the tape in motion causes the $S3$–W input (Fig. 22) to switch to the low state (while the pushbutton is depressed) and clears the output of Q601D to the low state.

Since the digital data may be read at any tape speed in the range 4·76 to 152·4 cm/s ($1\frac{7}{8}$ to 60 ips) the machine would normally be run at a high speed until the region of interest is reached. For precise location of the region of interest the tape machine could then be switched to a low speed (provided that the machine had been initially stopped a little "early").

Control signal T is coupled to NAND gate Q604D and inhibits the entry of any further time-of-day readings into the respective stores after it (T signal) switches to the low state. Thus the time display will be "frozen" while the tape machine comes to a stop.

Control signal I_{nx} (where $I_{nx} = T' + I_n'$) is used in conjunction with the selected data store (Section 3.9).

3.9 Selected Data and Fixed Data Store

In the table presented towards the beginning of Section 3.8 the encoding format for the time-of-day and the fixed data was indicated. All such data encoded in frames 0 and 1 (see table) are handled by the store discussed in Section 3.8 and the associated displays (Section 3.10). The remainder of the fixed data encoded in frames 2 and 3 includes month-of-the-year (1 to 12 in decimal) and run number (0000 to 9999 in decimal). Storage of these data together with those corresponding to any word as selected by a front panel mounted switch (Section 3.10) is provided by the "selected data and fixed data store".

Complete circuit details of the selected data and fixed data store are drawn in Figure 23.

Data outputs b_0 to b_{15} and parity checkbits p_1 and p_2 (p_2 not generated for parallel system) from the serial to parallel converter (Figs. 19 and 21) are buffered via inverters Q714A to Q716F before being coupled to the D inputs of the bistable latch stores (Fig. 23).

NAND buffers Q702A and Q702B invert the Y_3 and Y_4 inputs (discussed in Section 3.8) and provide sufficient drive capability to satisfy the clocking requirements of the bistable latch stores Q704 to Q708.

Fixed data comprising month-of-the-year information and the two most significant run number digits are entered into stores included in binary latches Q705 (two latches only), Q706, Q707 and Q708 at the time Y_3 (Section 3.8) switches low. Store outputs m_{27} to m_{40} are relevant here (but m_{32} is spare as indicated in the table towards the beginning of Section 3.8).

Fixed data comprising the two least significant run number digits are entered into stores included in binary latches Q705 (two latches only), Q704 and Q709 (two latches only) at the time Y_4 switches low. Store outputs m_{41} to m_{48} are relevant here.

Binary latches Q709 (two latches only), Q710, Q711, Q712 and Q713 are used for the storage of any word as selected via the front panel thumbwheel switches. Data are transferred to these stores when the input I_{nx} (Fig. 23) is low. As indicated in Section 3.8:

$$I_{nx} = T' + I_n'.$$

The timing relationship of I_n is indicated in Figures 14 and 18 for the serial and parallel systems respectively.

The encoding configuration for the selected word is summarized in the following table.

Serial to parallel converter output notation	Store output (selected word) designation
b_0	m_{49}
b_1	m_{50}
b_2	m_{51}
b_3	m_{52}
b_4	m_{53}
b_5	m_{54}
b_6	m_{55}
b_7	m_{56}
b_8	m_{57}
b_9	m_{58}
b_{10}	m_{59}
b_{11}	m_{60}
b_{12}	m_{61}
b_{13}	m_{62}
b_{14}	m_{63}
b_{15}	m_{64}
p_1	m_{65}
p_2	m_{66}

Because of the inversion performed on the input data (b_0, etc.) the $\bar{Q}$ outputs of the bistable latches, which make up the selected data and fixed data store, are used.

Outputs from the selected data and fixed data store of Figure 23 are taken to front panel displays detailed in Section 3.10. NAND buffers Q701A and Q701B act as drivers for parity lamps incorporated in the front panel display.

3.10 Front Panel Components

Data stored as detailed in Sections 3.8 and 3.9 may be displayed using numeric indicator units (Fig. 24*a*) mounted on the front panel. Each of these units (IU1 to IU20) comprises an indicator tube (V1 to V20), a binary-coded-decimal (BCD) to decimal decoder (Q1 to Q20), and a valve socket type connector (P141 to P160).

Decimal thumbwheel preset stop switch units (Fig. 24*b*) mounted on the front panel enable the "stop" point of the tape transport to be preset. Each of these switch units (SU1 to SU8) comprises a thumbwheel decoding switch (S4A to S4H) and a mating connector (P161 to P168). The switches require complementary inputs from the time-of-day store (Section 3.8) and eight diodes (Fig. 24*b*).

Connections to, and the relevance of, the various components which are mounted on the front panel are detailed in the associated document.[7]

3.11 Computer Interrupt Controller

Processing of the output data from the ground station digital interface is performed using a PDP 11 computer (manufactured by Digital Equipment Corporation) fitted with a type DR11A 16-bit general purpose input/output module. This module has two interrupt request lines. Normally one line would be used to interrupt the computer for data input and one for data output (on a 16-line output separate from the input lines). In this particular application the output of data from the computer internal processor to the DR11A is not a requirement, so both interrupt lines can be utilized for loading data into the computer from the interface. It has been found convenient to use one interrupt for new frame identification and the other to indicate when a new data word is ready.

When the interrupt is serviced the computer sends out a positive going pulse on the DATA TRANSMITTED (abbreviated DATA TRM in this text) line from the DR11A module. It is necessary for the ground station interface to terminate the present interrupt request when this pulse is generated to ensure that only one pass of the service routine is performed per frame or word interrupt.

To generate compatible interrupt request signals for the DR11A a Computer Interrupt Controller has been included. Circuit details of the board are given in Figure 25. Frame synchronizing signal N and read command signal I (Section 3.6) set the two D type flip-flops of Q802. The DATA TRM pulse received from the computer clears the flip-flop outputs N_C and I_C respectively. N_C and I_C constitute the frame and the word (or read command) interrupt outputs respectively and are coupled to the DR11A module. The interrupt requests become "true" when the outputs switch high. I_C and N_C are coupled to output connectors J103 and J113 (Appendix 4) via the buffer board (Appendix 3).

Data outputs b_0 to b_{15} (Figs. 19 and 21) suitably buffered (Appendix 3) are taken to the 16-line data input to the DR11A. These outputs are a true representation of the data only for a relatively short period, nominally while I is low. However, there is adequate time to enter the service routine even at the highest data rates. At present the parity outputs are not read by the computer.

NAND gate Q801D is not used in relation to the generation of computer interrupt signals; it generates a 4-FRAME SYNC output correctly timed for use in the reading of point-sampled FM data.

4. PERFORMANCE OF INTERFACE UNIT

To assess the performance of the ground station digital interface it has been first necessary to complete:

(i) airborne data processor[2] (for use in data acquisition);

(ii) plug-in digital recording amplifiers[9] for use with the airborne magnetic tape recorder;

(iii) plug-in digital reproducing amplifiers[5] for the analogue tape machine used to reproduce the airborne data;

(iv) software to allow the interface output data to be read into and processed by a digital computer;

(v) analogue demultiplexer to allow multiplexed data recorded using FM techniques to be demultiplexed using control signals derived from the interface;

(vi) tape control selector[8] to allow both the interface and the computer to control tape motion in the analogue magnetic tape reproducer.

Final versions of all of the above have been produced and fully tested. In all cases correct operation has been confirmed.

Only serial type digital recording has been employed up to the present; hardware for use with the parallel system of encoding has been completely validated with the tape recording function only omitted. Serial recording using the RZ format[5] has been adopted as the normal recording technique as only one tape track is required.

Flywheel techniques employed in the interface allow incoming data with bit repetition rates varying between 640 and 20,480 Hz (i.e. a 32 : 1 variation) to be read without the need for any component adjustments or the change of any switch settings.

By setting the tape machine preset stop switch (on the front panel of the interface) to the desired stop time the ability of the interface to stop the analogue tape motion at the prescribed time has been proven.

A computer program written in PAL 11 (assembly language for PDP 11 computer) source language allows the following to be realized:

(i) keyboard entry of time-of-day boundaries of selected block of data to be processed;

(ii) computer control of start, stop, rewind and tape speed of the analogue magnetic tape transport used to reproduce the recorded data;

(iii) entry of data into the central processor under interrupt control;

(iv) processing of the selected data and printout.

Reliable operation under the control of this program has been proven.

Photographs of the completed Ground Station Digital Interface are given in Figures 26 and 27.

5. REVIEW OF DATA REDUCTION SYSTEM

Since the time the manufacture of equipment described in this report was started many new components (integrated circuit devices, numeric displays, etc.) have become available commercially. With presently available components the circuit functions detailed herein could have been performed more simply and with reduced component count.

The flywheel gap detection techniques described herein enable a very broad input data rate to be accommodated without operator intervention. However, considerable care has to be exercised in the design and adjustment of the flywheel circuit to achieve optimum bandwidth. Correct operation over an extra octave (i.e. over a 64 : 1 range in lieu of 32 : 1) has been achieved but with increased sensitivity to noise at the higher data rates.

It would seem that word synchronization could be dispensed with (i.e. two-bit word gap inserted by the acquisition equipment could be eliminated) and frame synchronization only retained, particularly as there have been no observable problems with loss of synchronization with the present system of serial encoding.

By devoting one bit per data word plus one complete word for synchronization purposes a continuous data stream[2] without time gaps could be used. With such a system of serial encoding the electronic flywheel could probably be dispensed with, and at the same time a broader range of input data rates could be accommodated without operator intervention.

6. SUMMARY

Digital computer interface equipment has been developed and fully tested in operation. Principal features of the equipment include:

(*a*) time gaps in digitally encoded data are detected and digitized over a 32 : 1 range of bit rates using a flywheel circuit;

(*b*) time-of-day, date and run number information which are encoded using only one 16-bit word per frame of data are continually displayed with the interface;

(*c*) any 16-bit word in the data frame can be selected for display in octal format with the interface;

(*d*) an associated analogue magnetic tape reproducing machine can be stopped at a preset time selected by the interface;

(*e*) output data assembled as 16-bit words can be read into an associated digital computer under the control of interrupt request signals generated by the interface;

(*f*) control signals generated by the interface can be used to demultiplex analogue data recorded at the same time as the digital data on a separate magnetic tape track;

(*e*) Interface circuits are reliably protected against a 4% over-voltage by a trip circuit with "crowbar".

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3. Fraser, K. F.—Reduction Requirements for Data Acquired by an Airborne Data Logger. ARL Mech. Eng. Report 130, March 1971.
4. Telemetry Working Group of the Inter Range Instrumentation Group—Telemetry Standards. IRIG Document No. 106-69, February 1969.
5. Fraser, K. F., and Krieser, U. R.—Digital Reproducing Amplifiers for a Magnetic Tape Recorder. ARL Mech. Eng. Note 337, September 1972.
6. Fraser, K. F., and Krieser, U. R.—Serial Digital Data Generator. ARL Mech. Eng. Note 327, July 1971.
7. Krieser, U. R.—Ground Station Digital Interface System Detail. ARL Mech. Eng. Tech. Memo. 403, September 1980.
8. Krieser, U. R.—Remote Control for Tape Machine. To be published.
9. Fraser, K. F., and Krieser, U. R.—Digital Recording Amplifiers for a Magnetic Tape Recorder. ARL Mech. Eng. Note 326, June 1971.

APPENDIX 1

Component Identification

Components used on printed circuits and elsewhere have been given an identification label consisting of a letter prefix followed by a number comprising up to three digits. The letter prefix identifies the class of component as indicated in the following table.

Class of component	Letter prefix
Resistor	R
Capacitor	C
Transformer	L
Diode	CR
Transistor or Integrated Circuit	Q
Switch	S
Numeric Indicator Valve	V
Relay	K
Heatsink	HS
Test Point	TP
Terminal	TM
Terminal Board	TB
Indicator Lamp	LP
Chassis-mounted Connector	J
Cable Mounted Connector or Edge Connector Contacts on Printed Circuit Board	P

Resistance and capacitance values marked on the circuit diagrams are respectively in ohms and picofarad.

APPENDIX 2

System Details Under Separate Cover

Additional system details excluded from this report are contained in another paper,[7] the contents of which are summarized below.

1. Introduction
2. Circuit Details.
3. Operating Instructions.
4. Interwiring Details.
   - 4.1 Power Distribution.
   - 4.2 Wiring to Front Panel Mounted Components (excluding Connectors).
   - 4.3 Wiring to Front Panel and Rear Panel Mounted Connectors.
   - 4.4 Wiring to Printed Circuit Card Edge Connectors.
5. Component Identification.
6. Integrated Circuit Wiring Details.
7. Component Lists.
   - 7.1 Components for AC to DC Converter.
   - 7.2 Components for Voltage Regulators.
   - 7.3 Components for Output Buffers.
   - 7.4 Components for Input Clock Signal Generator.
   - 7.5 Components for Electronic Flywheel.
   - 7.6 Components for Control Signal Generator for Serial System.
   - 7.7 Components for Control Signal Generator for Parallel System.
   - 7.8 Components for Serial to Parallel Converter for Serial System.
   - 7.9 Components for Serial to Parallel Converter for Parallel System.
   - 7.10 Components for Time-of-Day Store and Preset Stop Generator.
   - 7.11 Components for Selected Data and Fixed Data Store.
   - 7.12 Components for Computer Interrupt Controller.
   - 7.13 Components for Front and Rear Panels and Chassis.
8. Output Connection Details.

APPENDIX 3

Output Buffer Connection Details

The output buffer (Fig. 7) has an input designated q_n and outputs as q_{nF} (interwired to front panel connectors) and q_{nR} (interwired to rear panel connectors) where $1 \leqslant n \leqslant 28$. The insertion of an appropriate link associated with each buffer stage determines whether the q_n input signal will be inverted or not as it passes through the buffer. If the "A" position of the link is chosen (Fig. 7) then logically

$$q_{nF} = q_{nR} = q_n,$$

whereas if the "B" position of the link is chosen

$$q_{nF} = q_{nR} = \bar{q}\bar{n}.$$

Details of the required link connections together with other relevant information are given in the following table.

Buffer output signal identifier*	Link position	Signal description
q_1	B	FM CLK
q_2	A	N_C (FRAME INT)
q_3	A	m_{14} (2-SEC SYNC)
q_4	B	4-FRAME SYNC
q_5	B	T (TAPE MACHINE PRESET STOP)
q_6	A	b_3 (BIT 3)
q_7		Spare
q_8		Spare
q_9	A	b_{13} (BIT 13)
q_{10}	A	b_{12} (BIT 12)
q_{11}	A	b_{14} (BIT 14)
q_{12}	A	b_{15} (BIT 15—LSB)
q_{13}	A	b_0 (BIT 0—MSB)
q_{14}	A	b_7 (BIT 7)
q_{15}	A	b_2 (BIT 2)
q_{16}	A	b_1 (BIT 1)
q_{17}	A	I_C (WORD INT)
q_{18}	A	m_{10} (20-SEC SYNC)
q_{19}	A	p (PARITY CHECKBIT)
q_{20}	A	m_7 (2-MIN SYNC)
q_{21}	A	b_6 (BIT 6)
q_{22}	A	b_5 (BIT 5)
q_{23}	A	b_8 (BIT 8)
q_{24}	A	DATA TRANSMITTED (input)
q_{25}	A	b_{10} (BIT 10)
q_{26}	A	b_9 (BIT 9)
q_{27}	A	b_4 (BIT 4)
q_{28}	A	b_{11} (BIT 11)

* The "F" (front panel) and "R" (rear panel) subscripts are omitted from the output identifiers in this table.

APPENDIX 4

External Signal Connections

Input/output connections to the interface may be made via connectors mounted at the front (Fig. 26) and rear (Fig. 27) of the instrument. The functions of the relevant connectors are summarized in the following table.

Connector	Location	Application
J101	Front panel	Digital signal input
J102	Front panel	Tape machine preset stop output (OUTPUT 1)
J103	Front panel	Digital computer output (OUTPUT 2)
J110	Rear panel	Mains input
J111	Rear panel	Digital signal input
J112	Rear panel	Tape machine preset stop output (OUTPUT 1)
J113	Rear panel	Digital computer output (OUTPUT 2)

Signal connections may be made either to connectors J101 to J103 on the front panel or to connectors J111 to J113 on the rear panel. Although the outputs to front and rear panel connectors are independently buffered the signals are identical.

Detailed information on the interwiring of the interface is given in the associated document.[7]

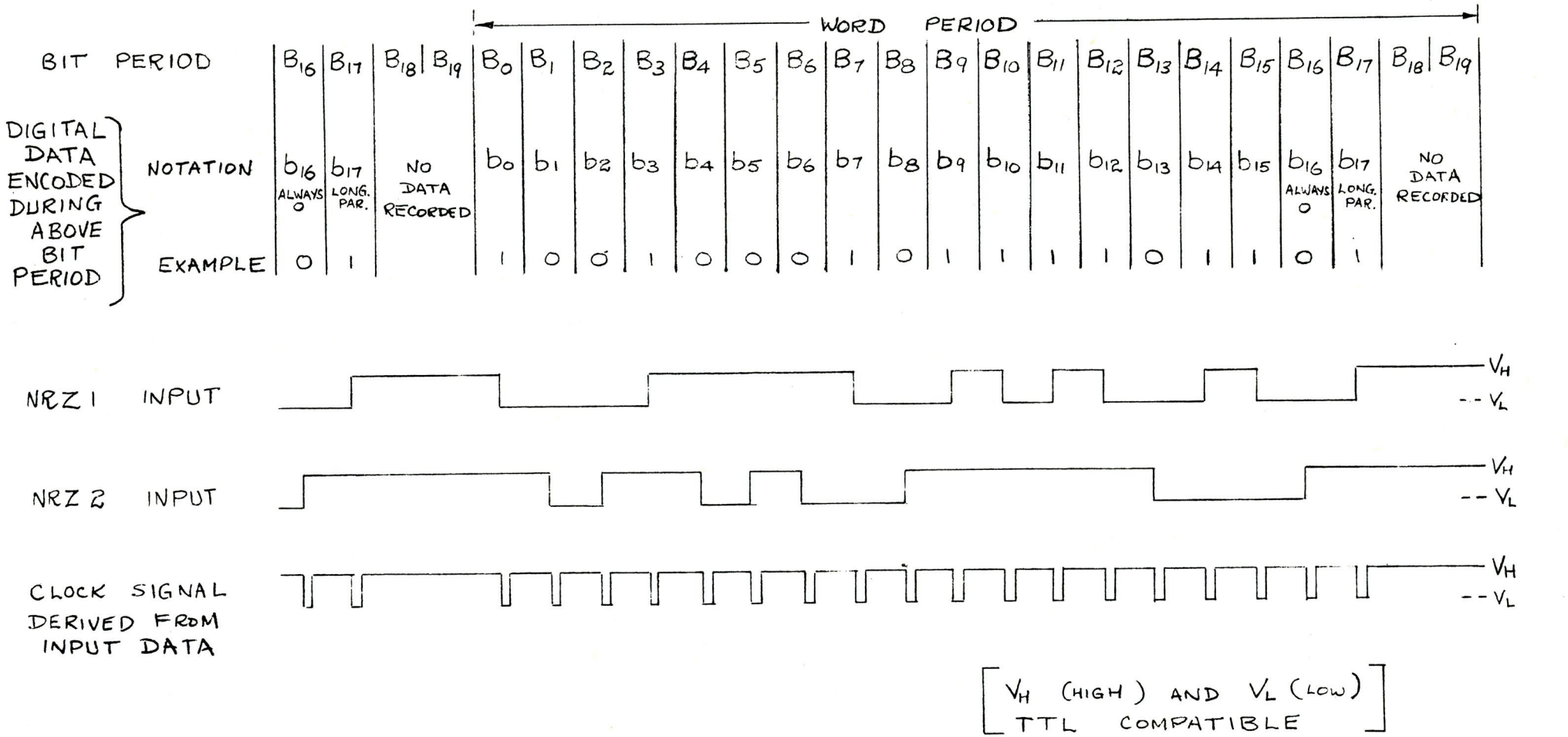


FIG. 1 TYPICAL INPUTS OVER ONE WORD PERIOD FOR SERIAL SYSTEM

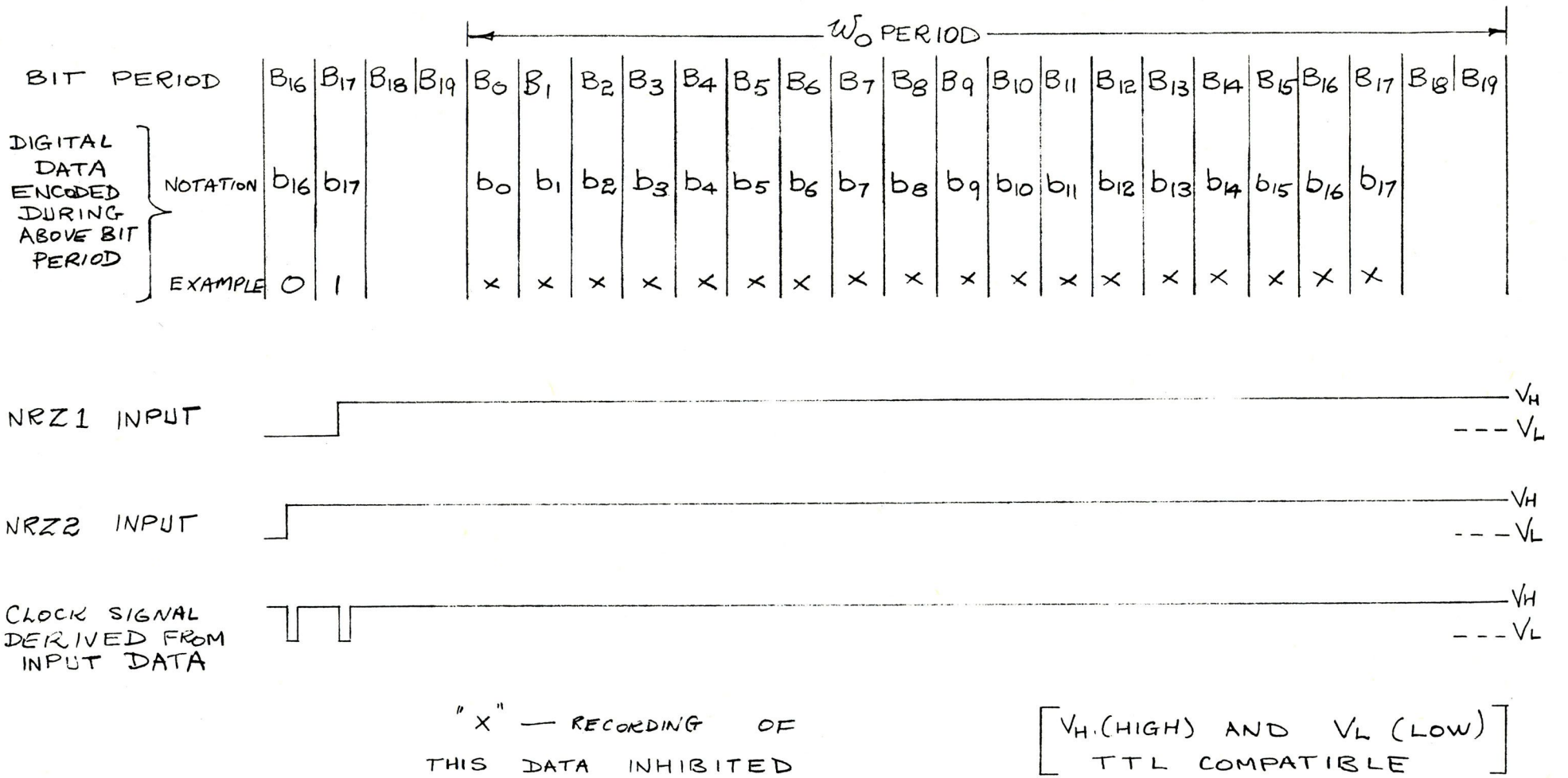


FIG. 2 FRAME SYNCHRONIZATION (TYPE A) FOR SERIAL SYSTEM

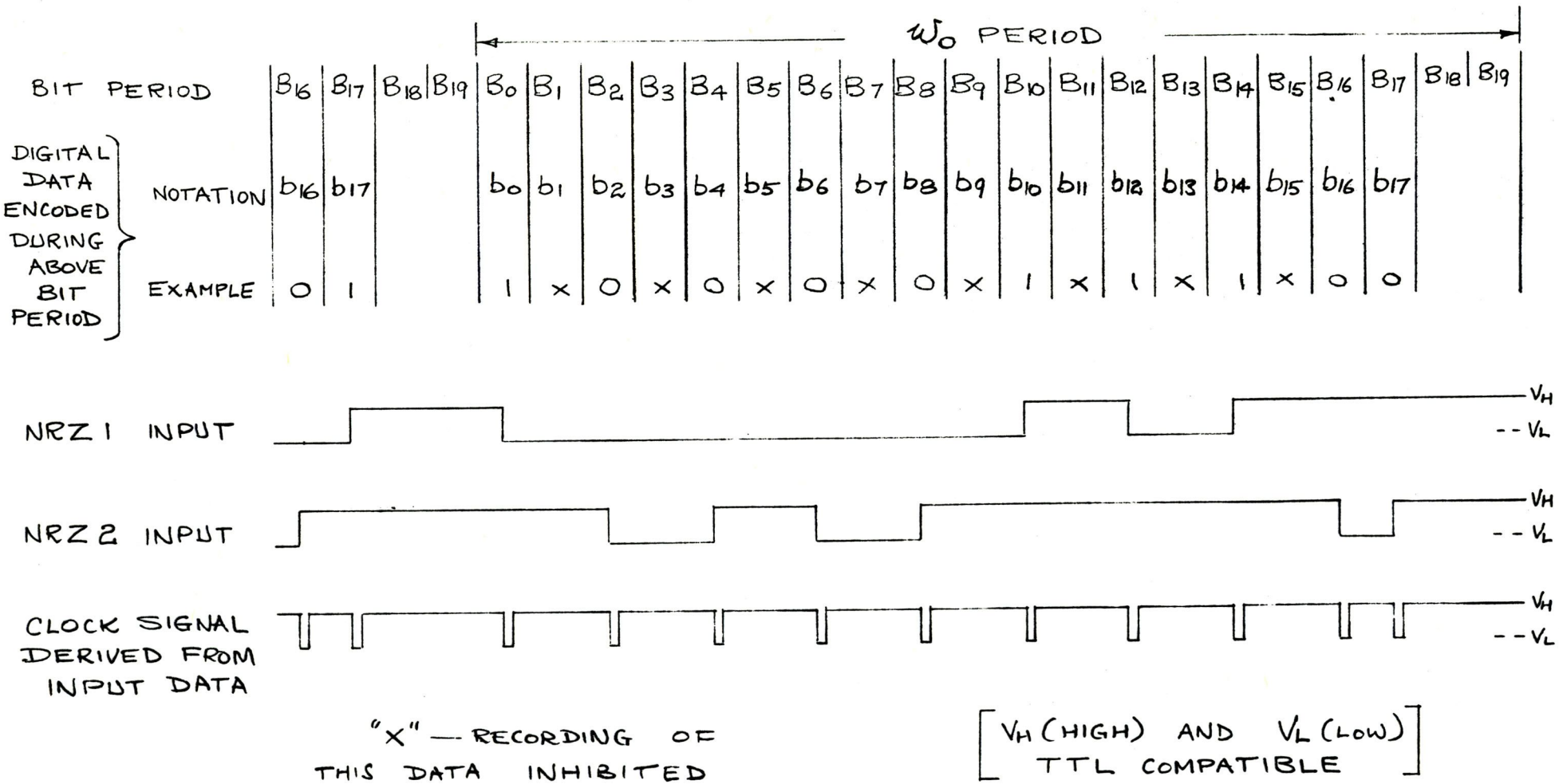


FIG. 3 FRAME SYNCHRONIZATION (TYPE B) FOR SERIAL SYSTEM

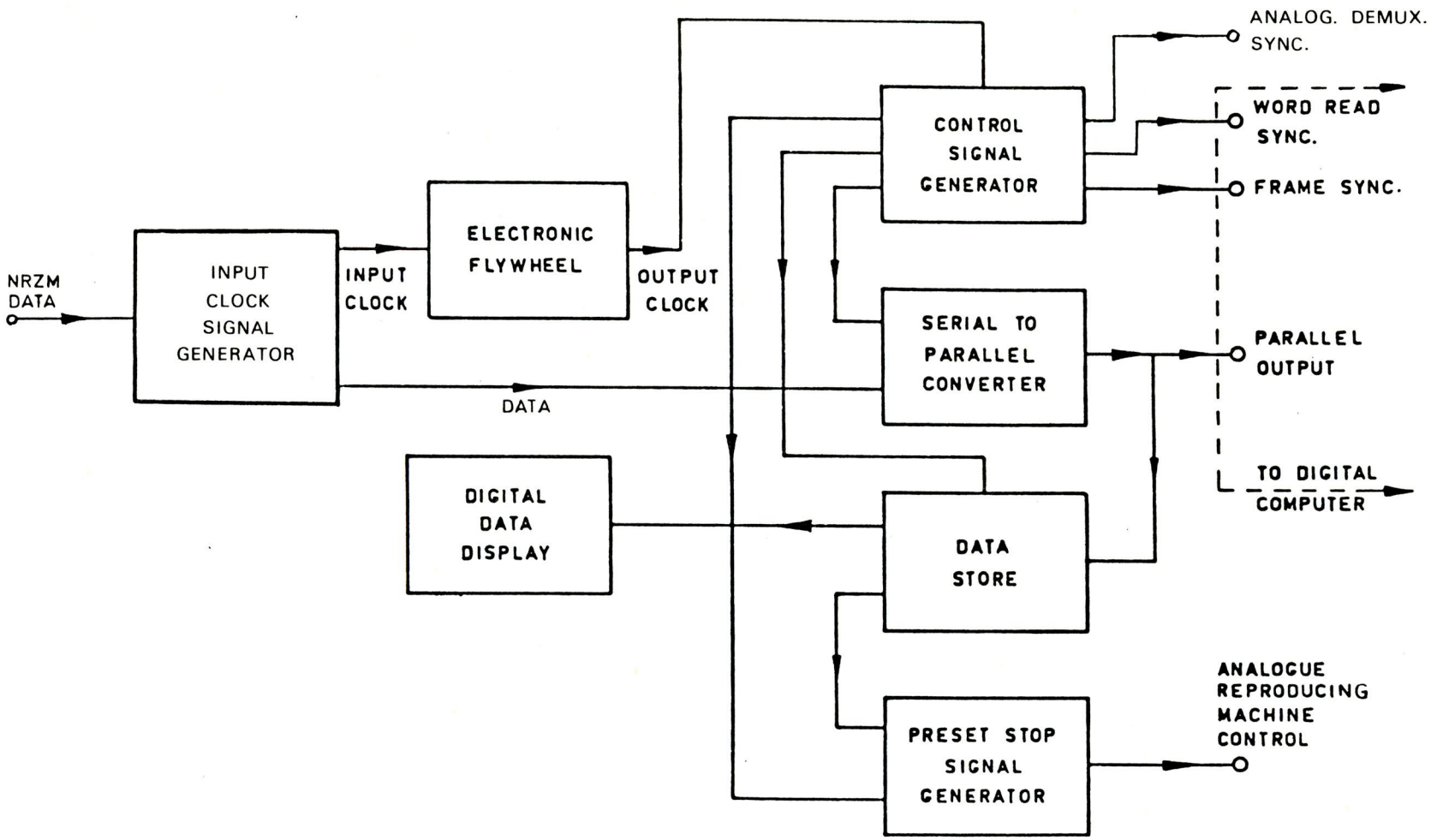


FIG. 4 BLOCK SCHEMA OF DIGITAL INTERFACE

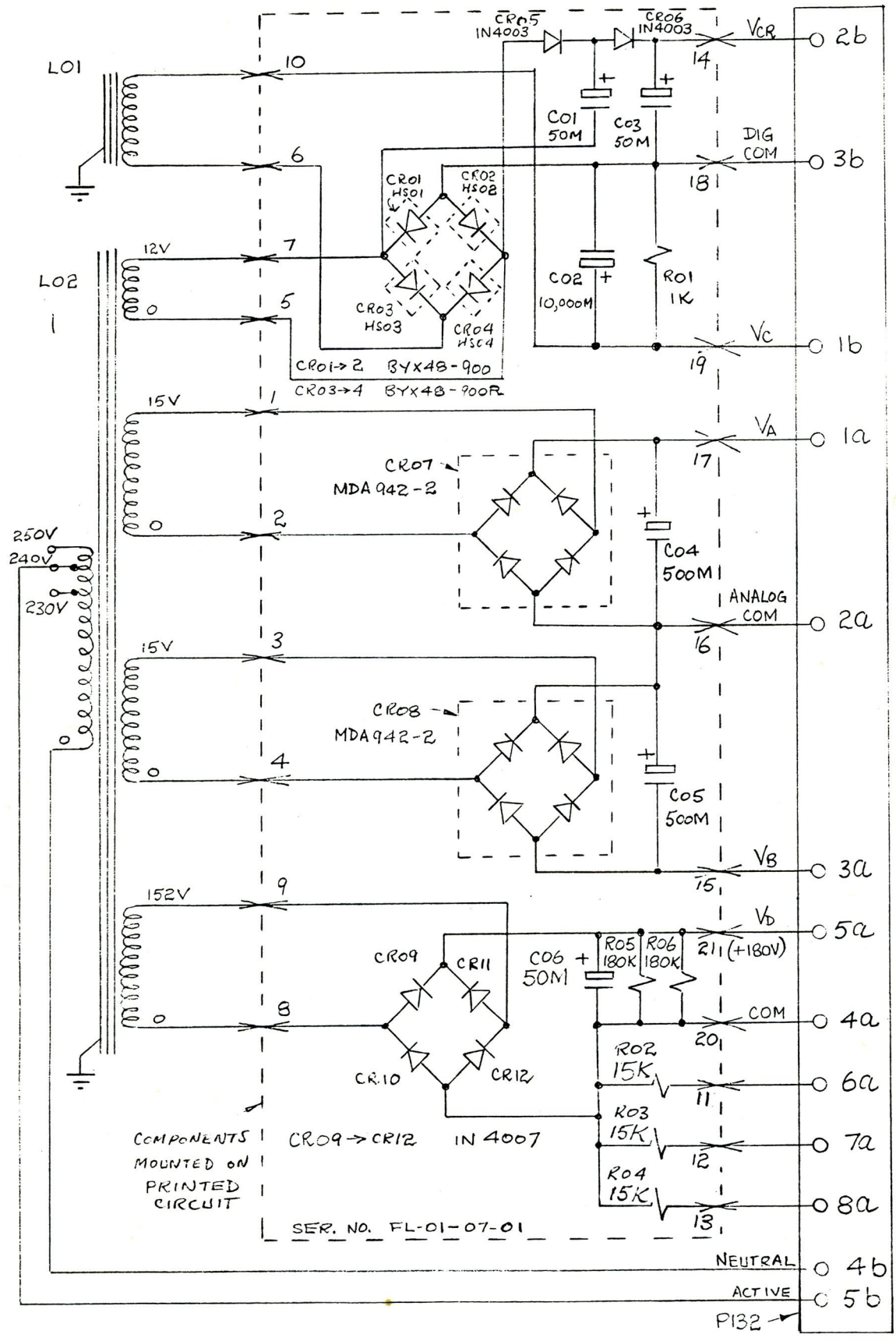


FIG. 5 AC TO DC CONVERTER

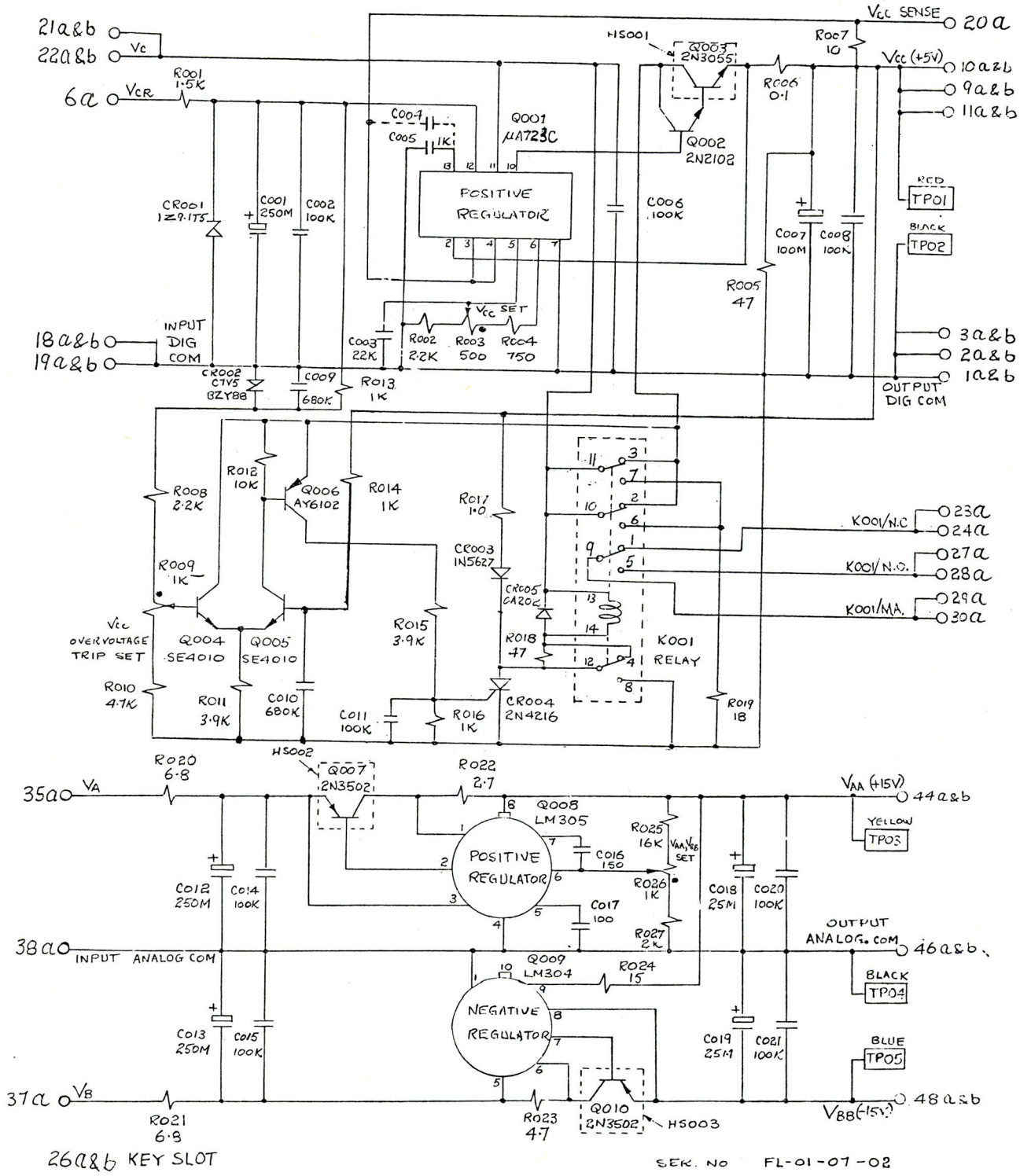


FIG. 6 VOLTAGE REGULATORS

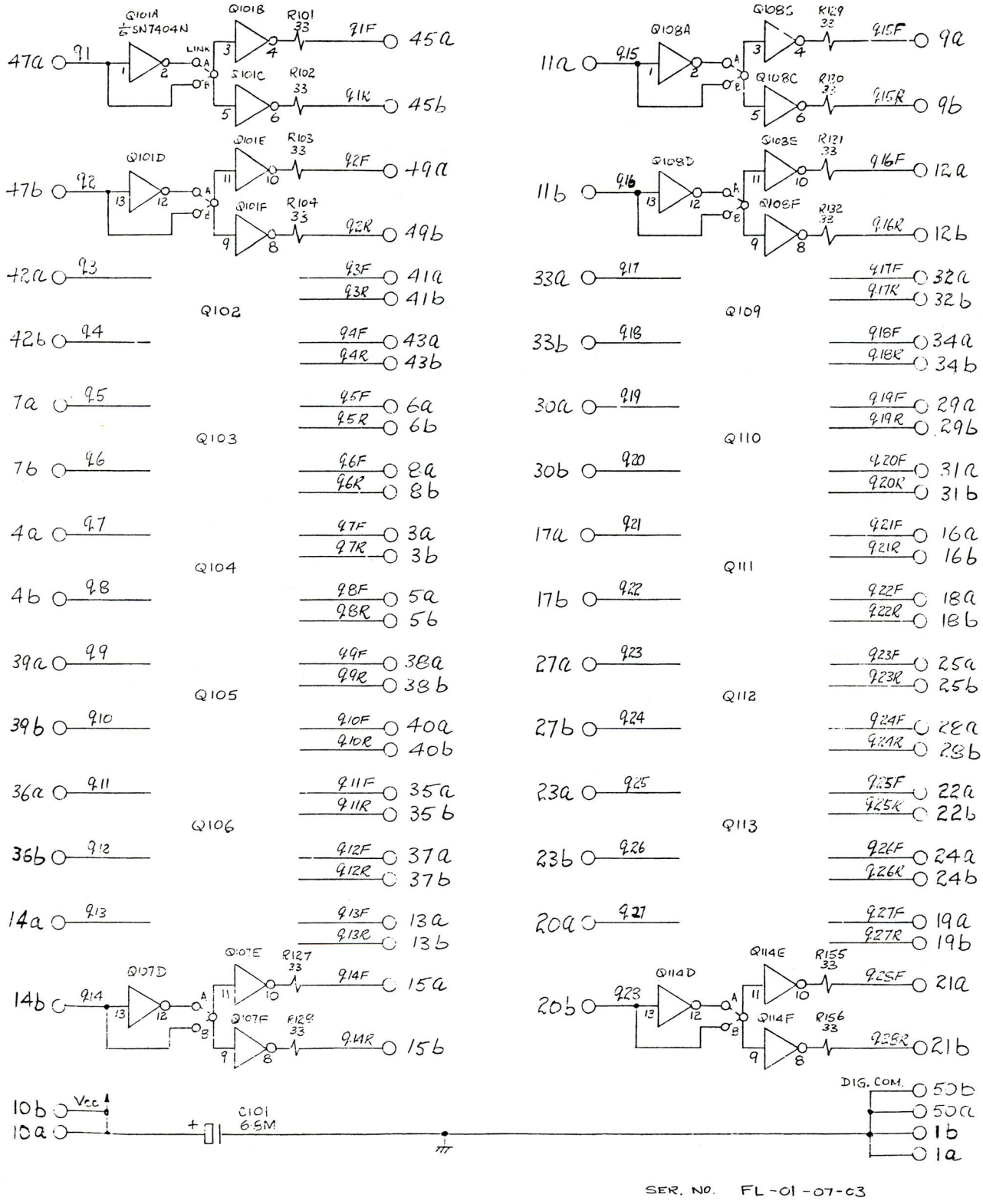


FIG. 7 OUTPUT BUFFERS

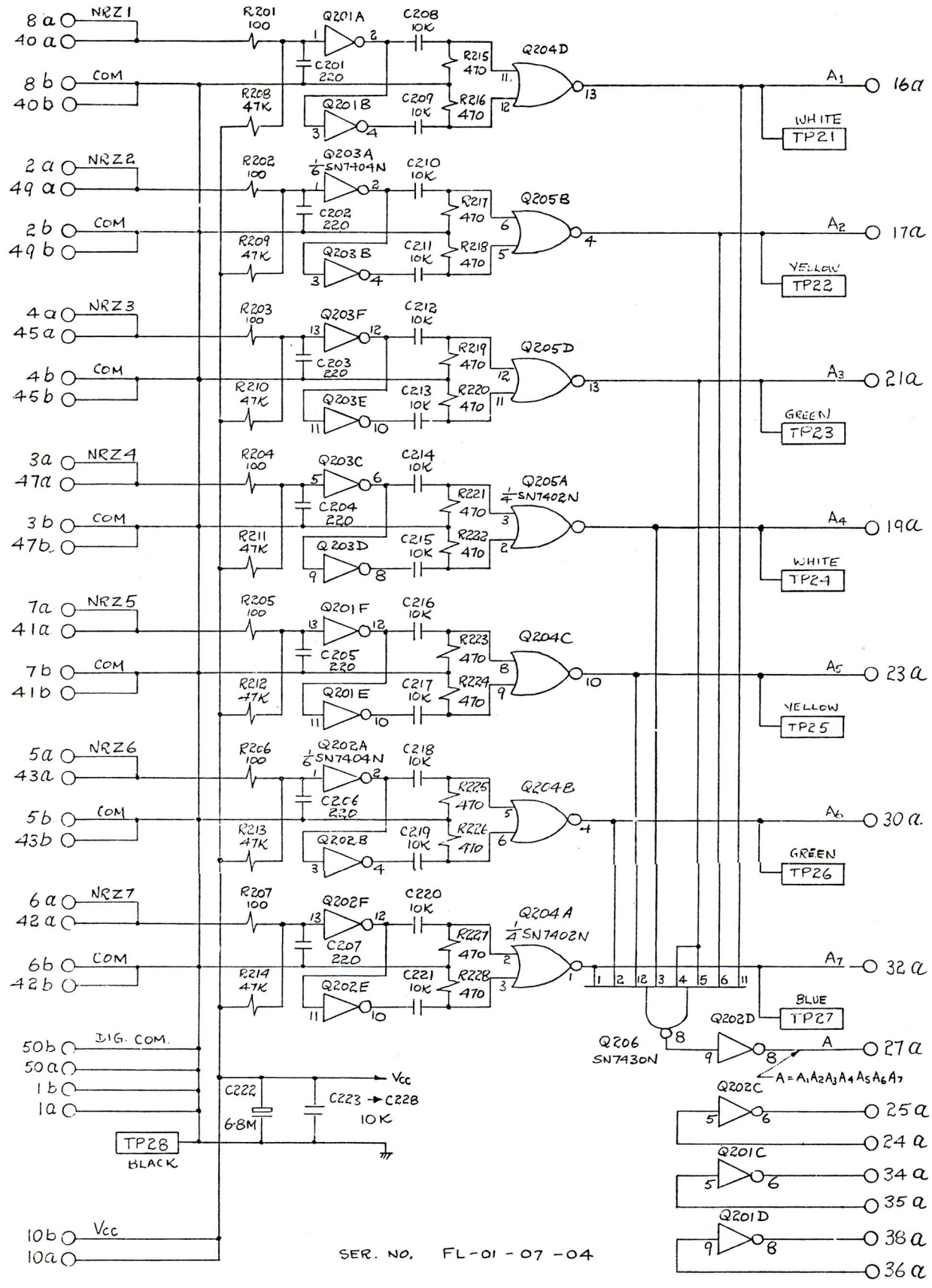


FIG. 8 INPUT CLOCK SIGNAL GENERATOR

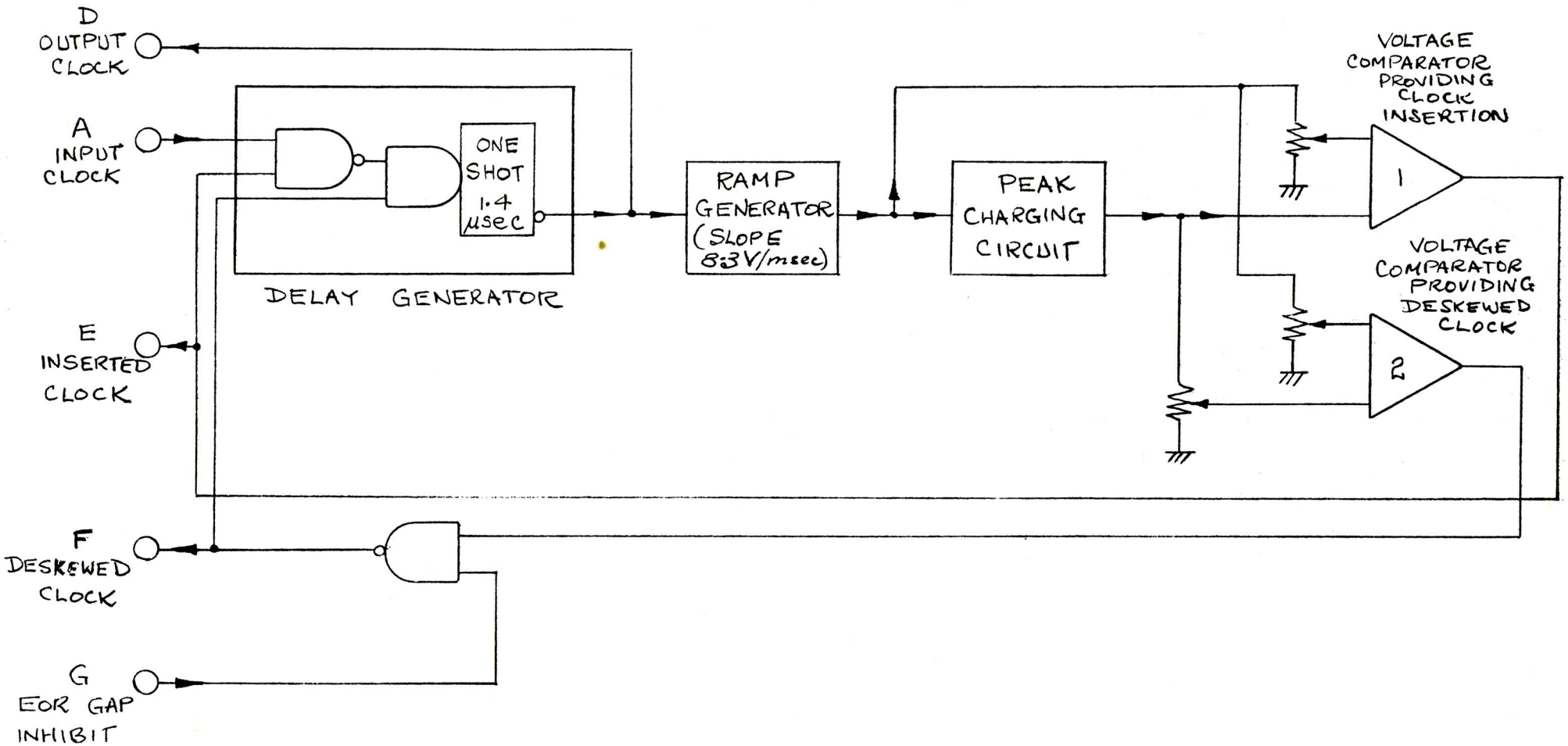


FIG. 9 BLOCK SCHEMA OF THE ELECTRONIC FLYWHEEL

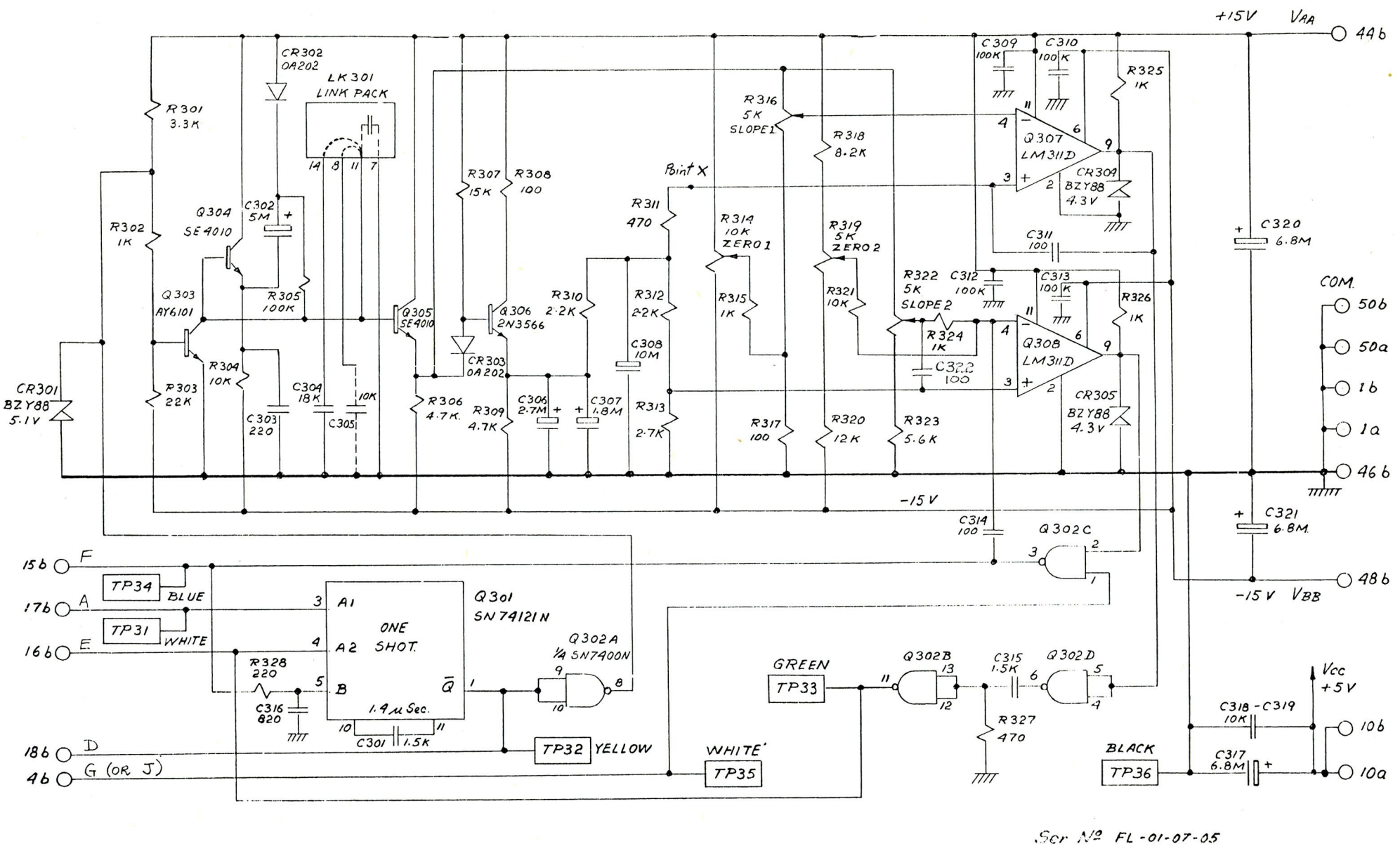


FIG. 10 ELECTRONIC FLYWHEEL

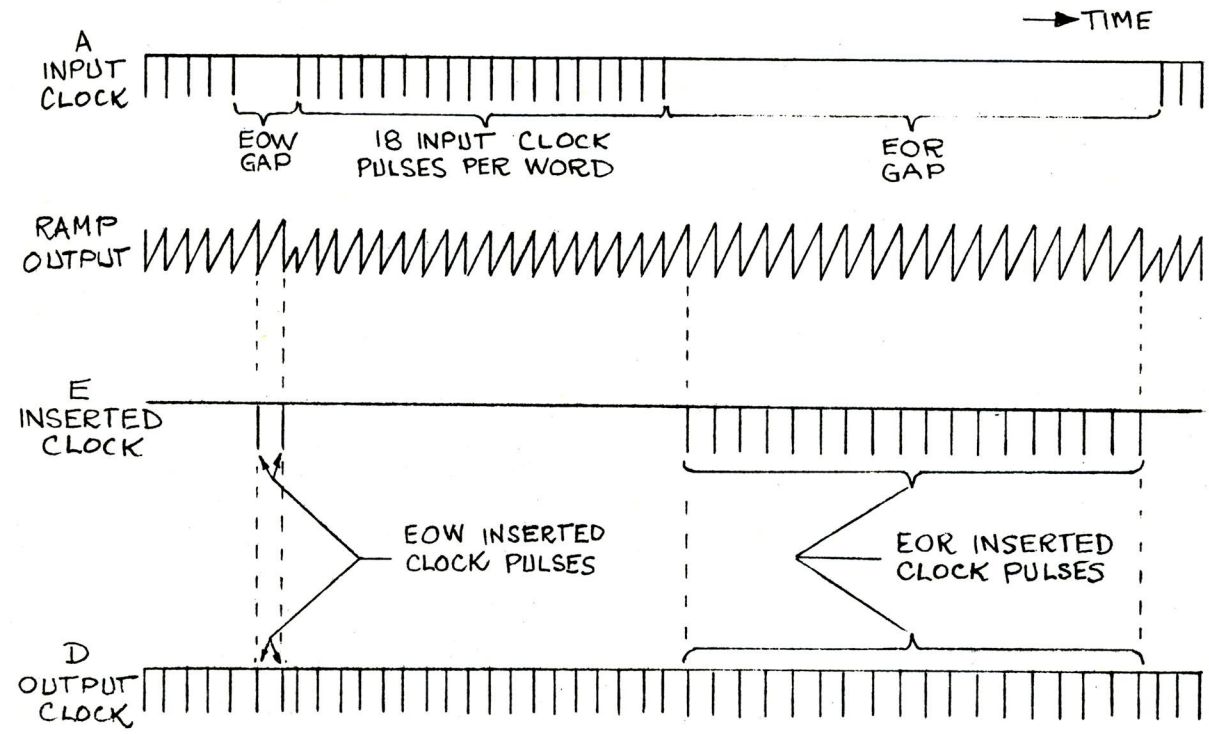


FIG. 11(a) ELECTRONIC FLYWHEEL WAVEFORMS FOR SERIAL SYSTEM EMPLOYING FRAME SYNCHRONIZATION TYPE A

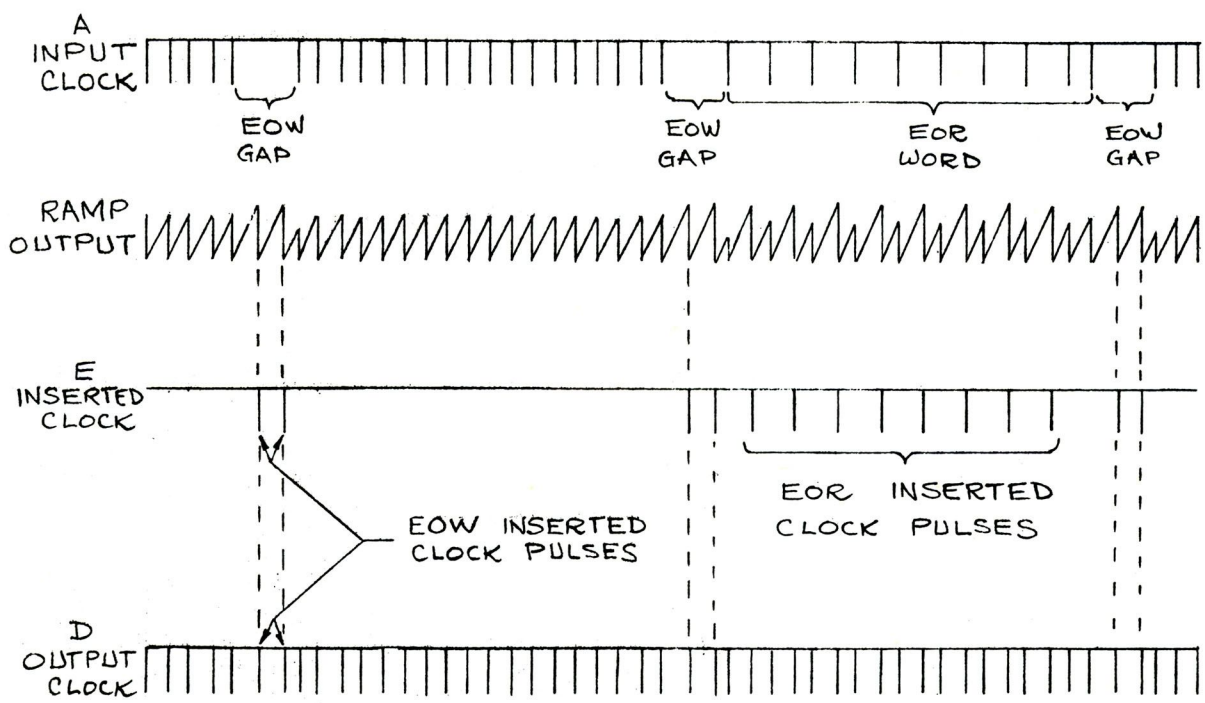


FIG. 11(b) ELECTRONIC FLYWHEEL WAVEFORMS FOR SERIAL SYSTEM EMPLOYING FRAME SYNCHRONIZATION TYPE B

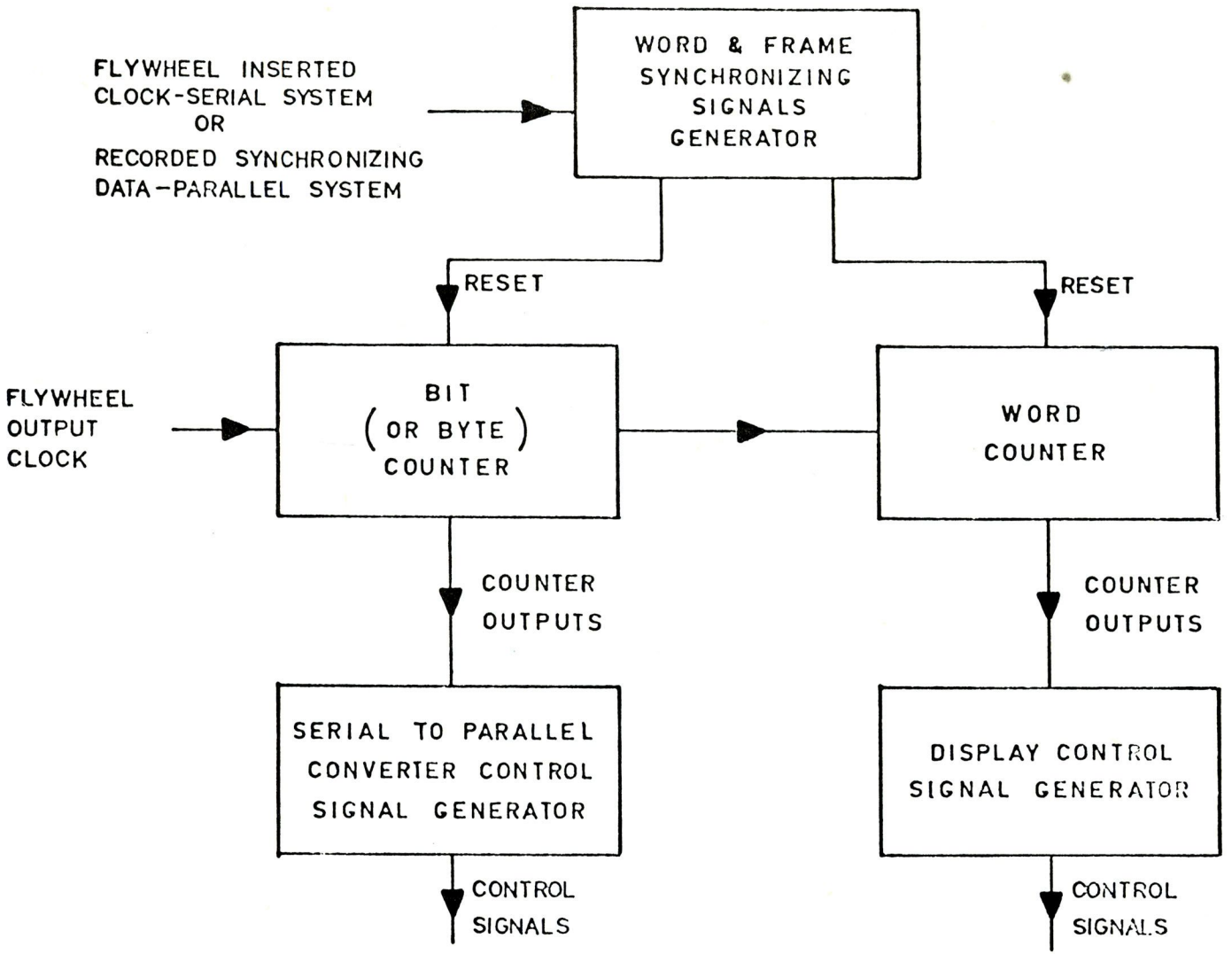


FIG. 12 BLOCK SCHEMA FOR CONTROL SIGNAL GENERATOR FOR SERIAL OR PARALLEL SYSTEMS

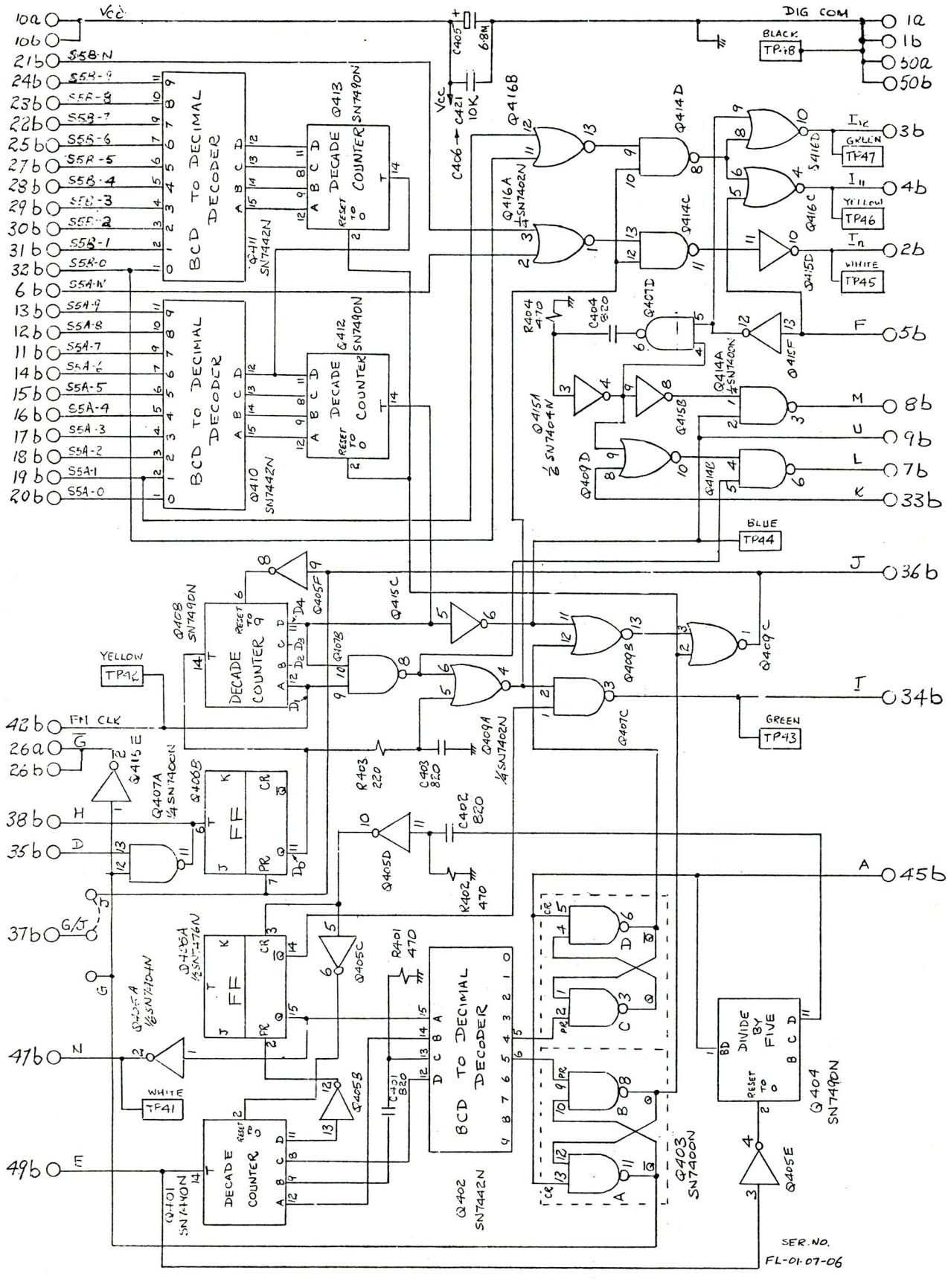


FIG. 13 CONTROL SIGNAL GENERATOR FOR SERIAL SYSTEM

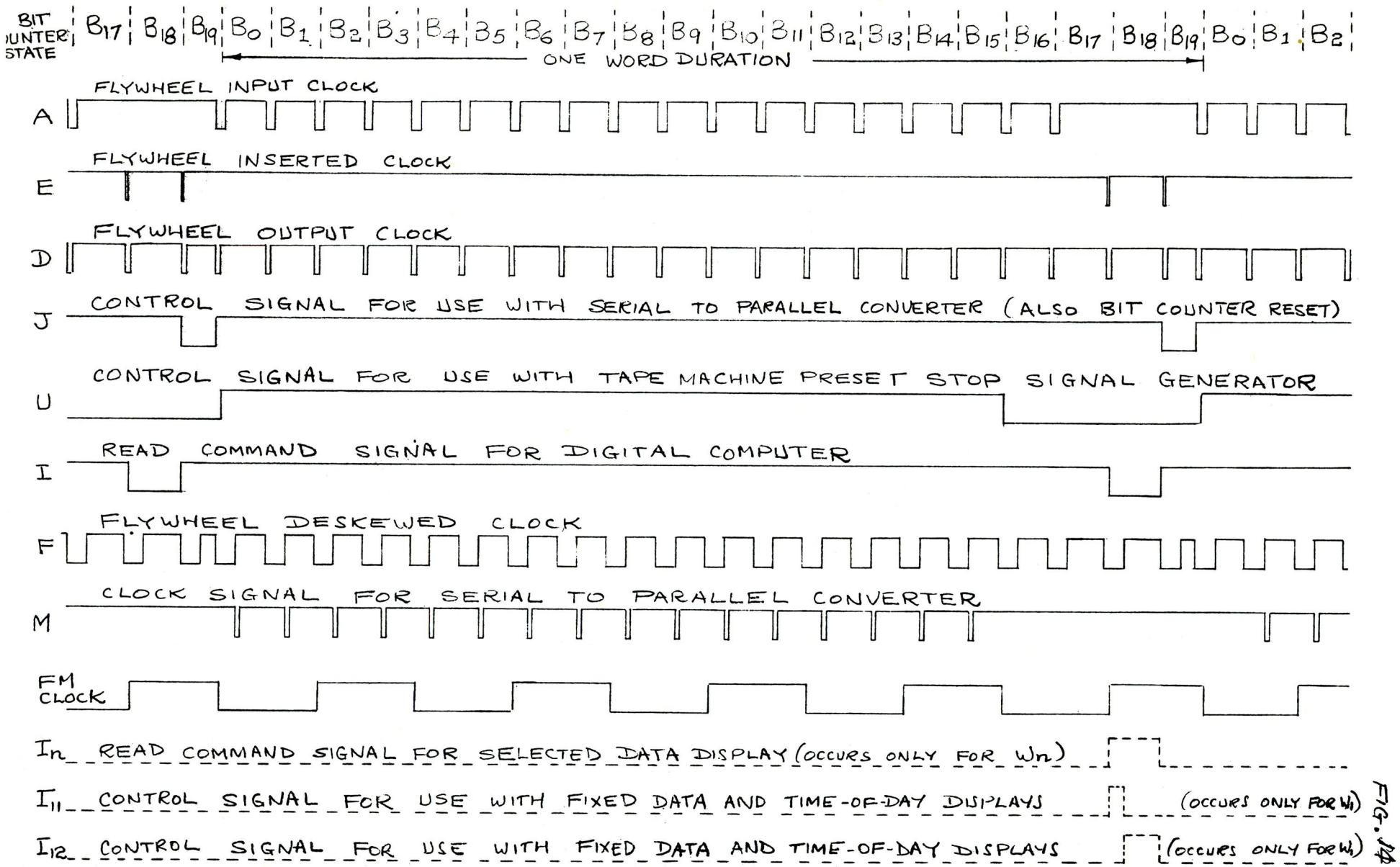


FIG. 14 TIME RELATIONSHIP OF CONTROL SIGNALS FOR SERIAL SYSTEM (FOR ANY WORD EXCEPT W_0)

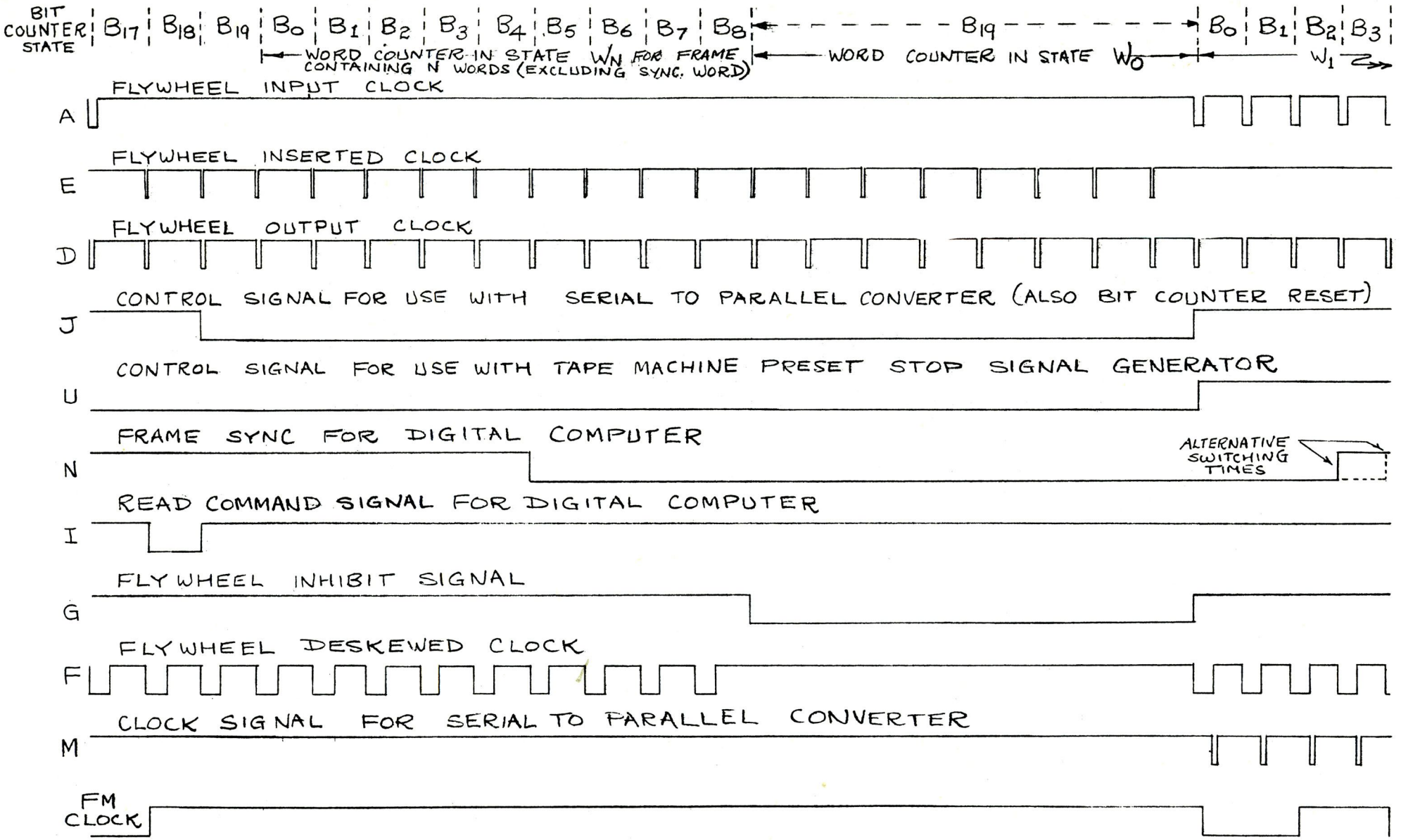


FIG. 15 TIME RELATIONSHIP OF CONTROL SIGNALS FOR SERIAL SYSTEM DURING SYNC. WORD WHEN FRAME SYNCHRONIZATION TYPE A IS USED

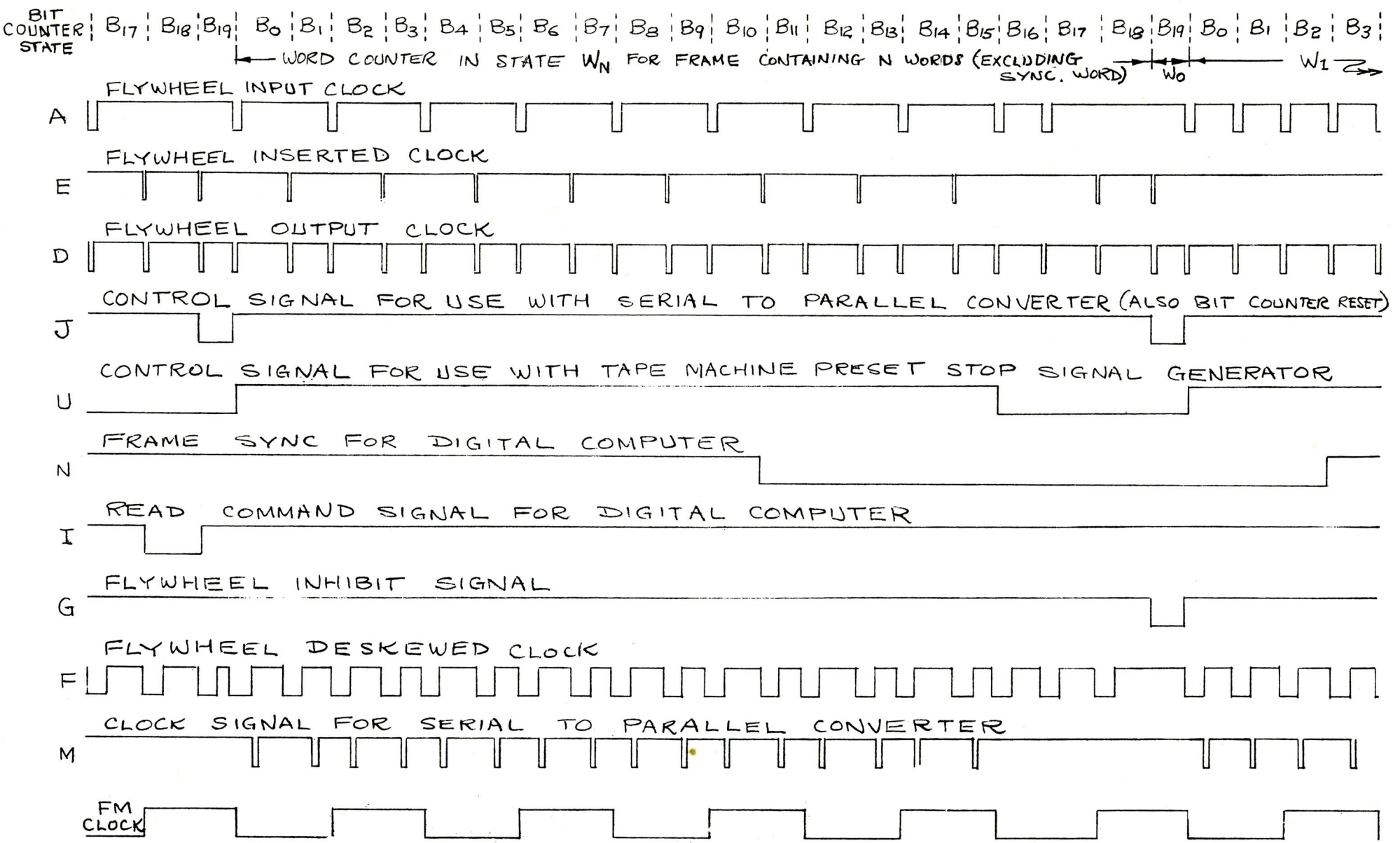


FIG. 16 TIME RELATIONSHIP OF CONTROL SIGNALS FOR SERIAL SYSTEM DURING SYNC. WORD WHEN FRAME SYNCHRONIZATION TYPE B IS USED

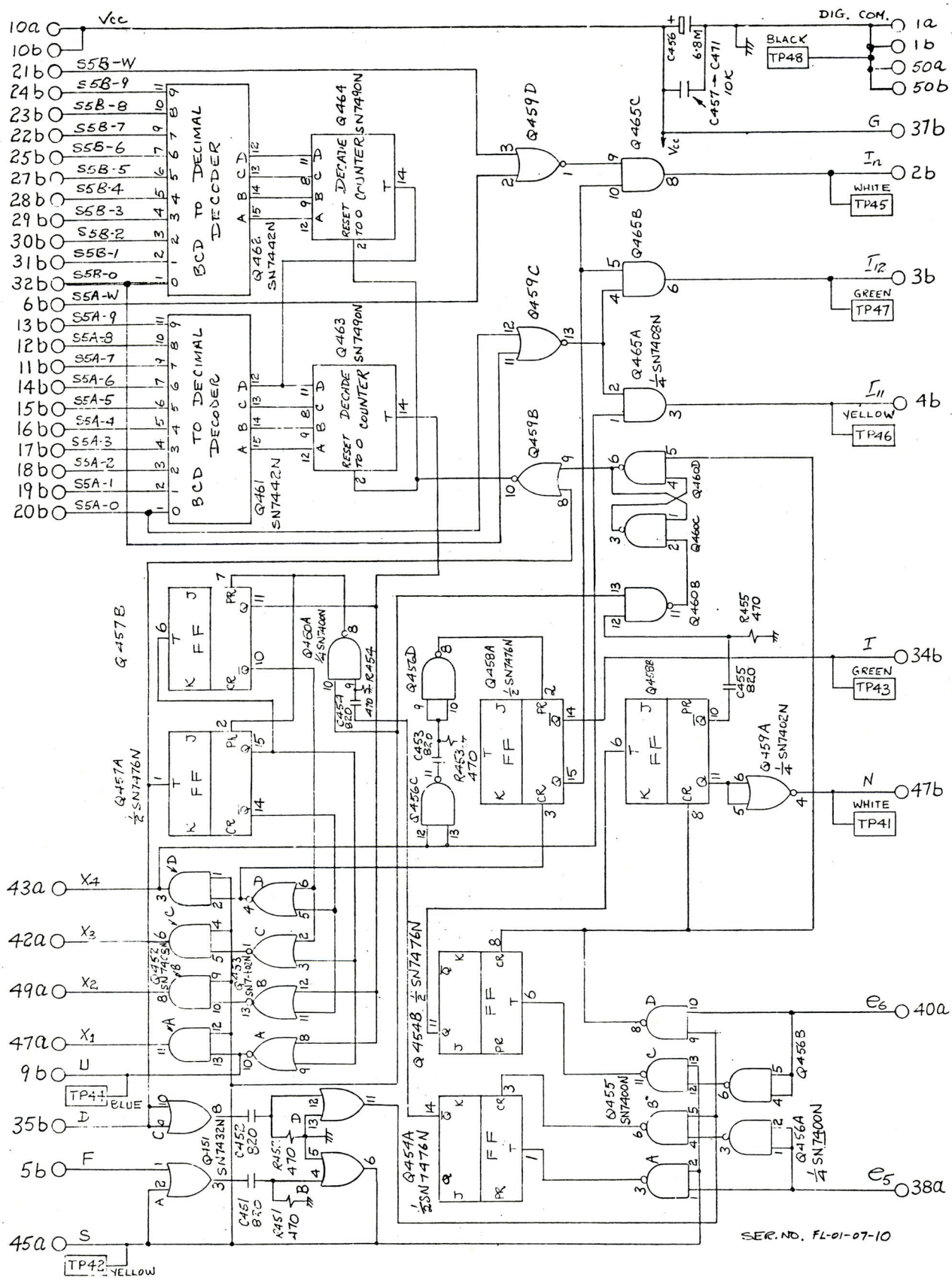


FIG. 17 CONTROL SIGNAL GENERATOR FOR PARALLEL SYSTEM

FIG. 18

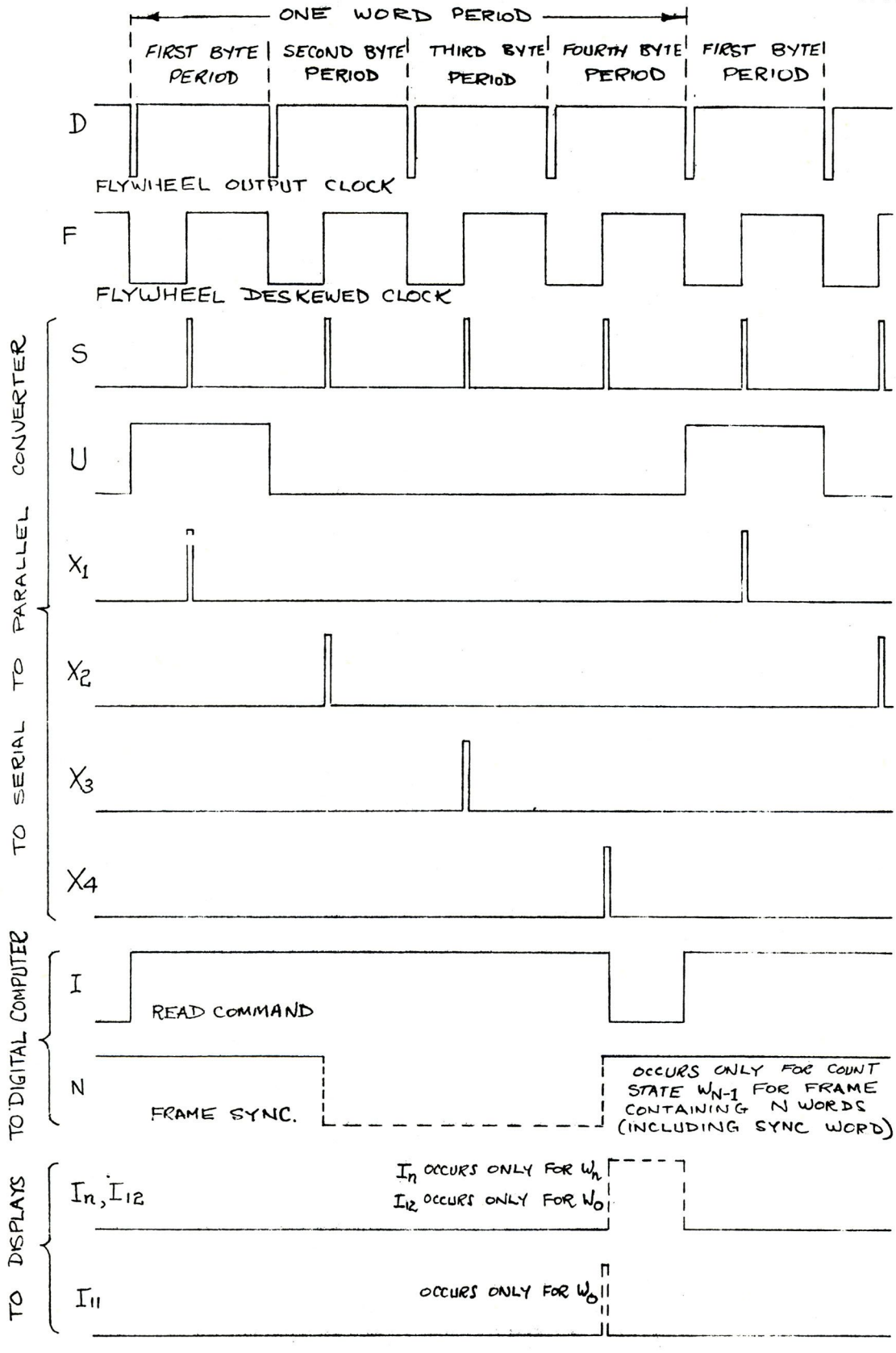


FIG. 18 TIME RELATIONSHIP OF VARIOUS CONTROL SIGNALS FOR PARALLEL SYSTEM

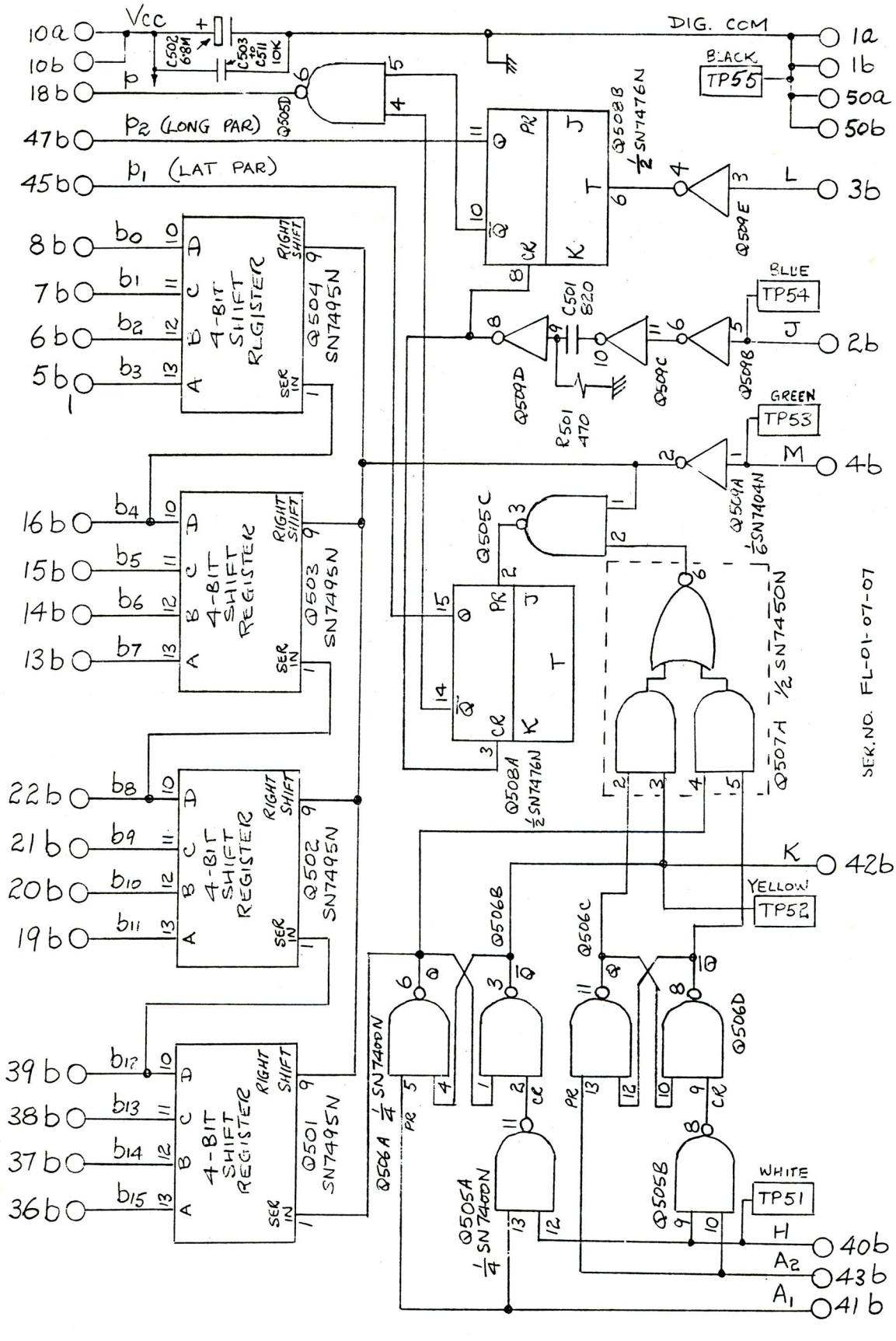
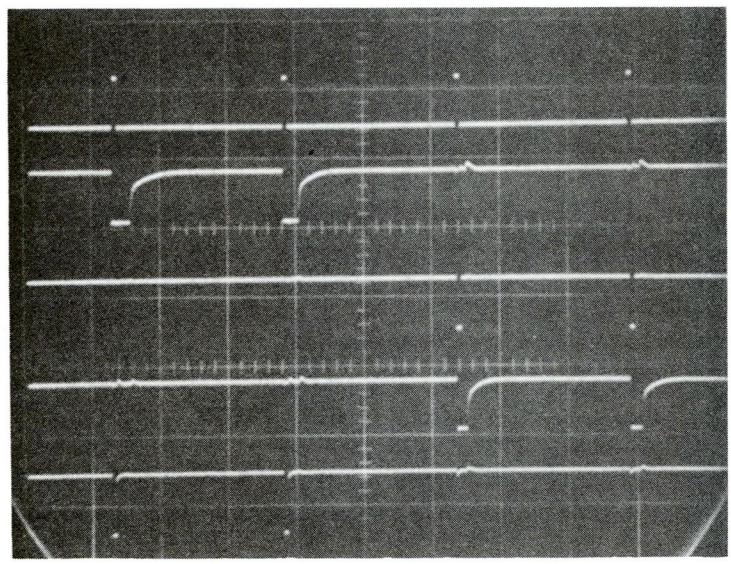


FIG. 19 SERIAL TO PARALLEL CONVERTER FOR SERIAL SYSTEM



(1) Clock H

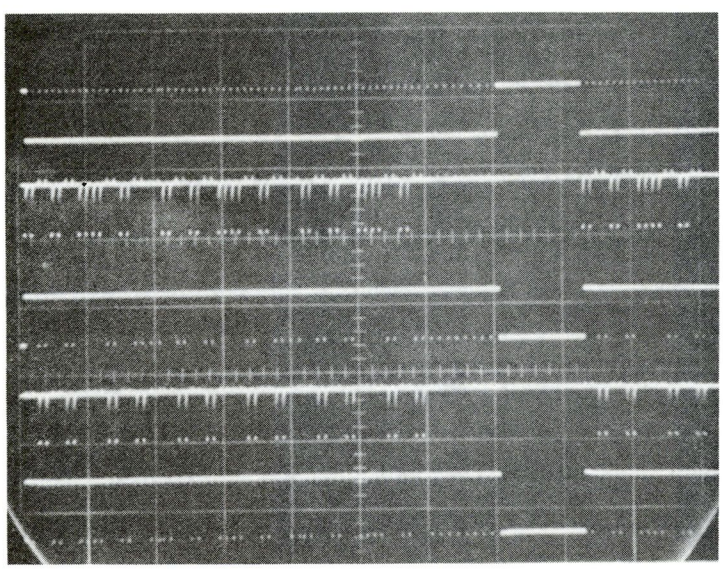
(2) Input A_1

(3) Clear input $(A_1H)'$

(4) Input A_2

(5) Clear input $(A_2H)'$

(a) Input waveforms obtained when reading digital information 1100 (part of word) for bit rate of 20.48 kHz



(1) Clock H

(2) Input A_1

(3) Clear input $(A_1H)'$

(4) Input A_2

(5) Clear input $(A_2H)'$

(b) Input waveforms obtained when reading repeated digital word 1100110011110011 00 for bit rate of 20.48 kHz and including EOR gap (for frame synchronization Type A)

FIG. 20 OSCILLOSCOPE TRACES OF INPUTS TO TEMPORARY STORAGE BISTABLES (DERIVED FROM Q506) USED IN SERIAL TO PARALLEL CONVERTER (FOR SERIAL SYSTEM)

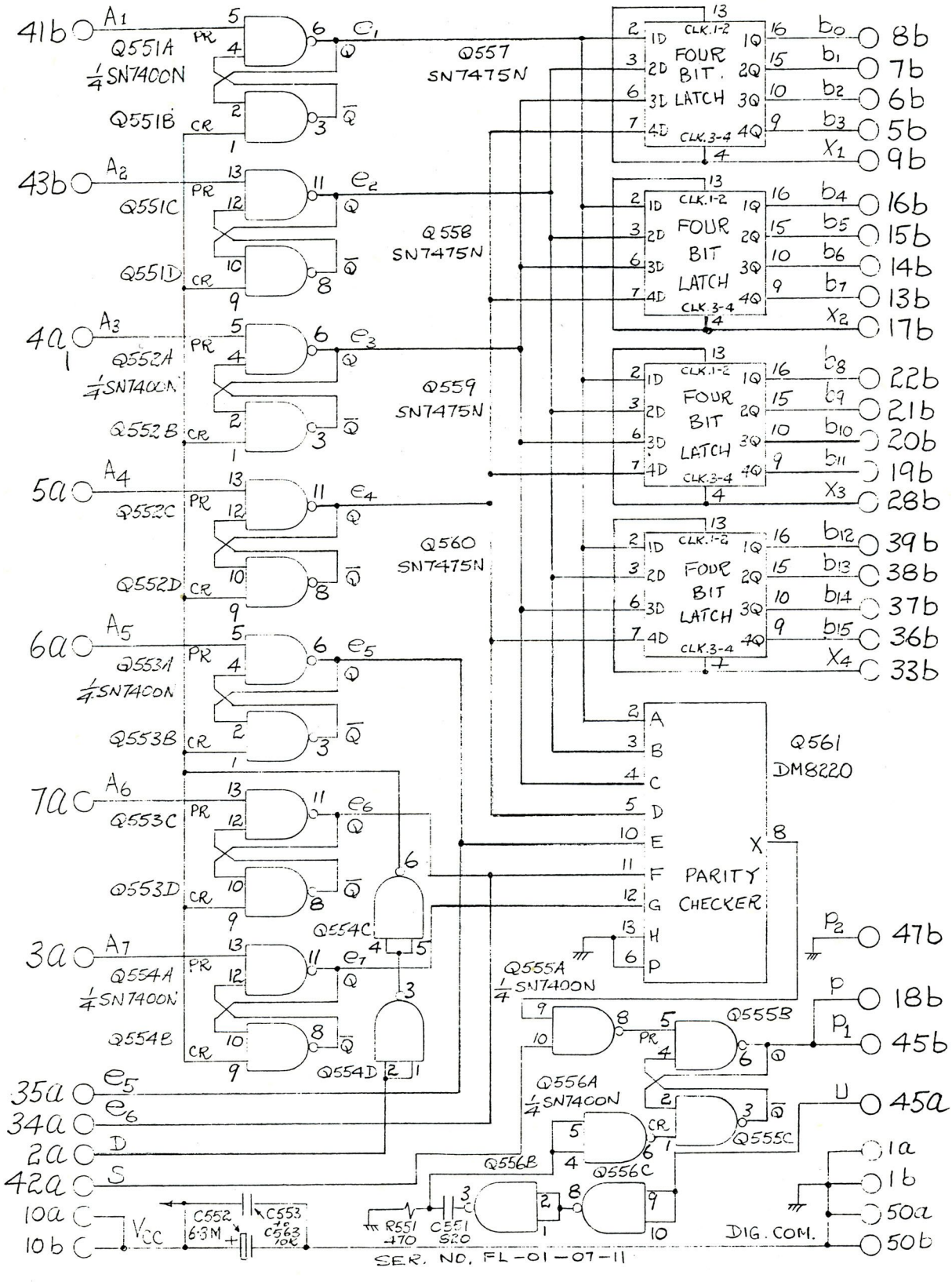


FIG. 21 SERIAL TO PARALLEL CONVERTER FOR PARALLEL SYSTEM

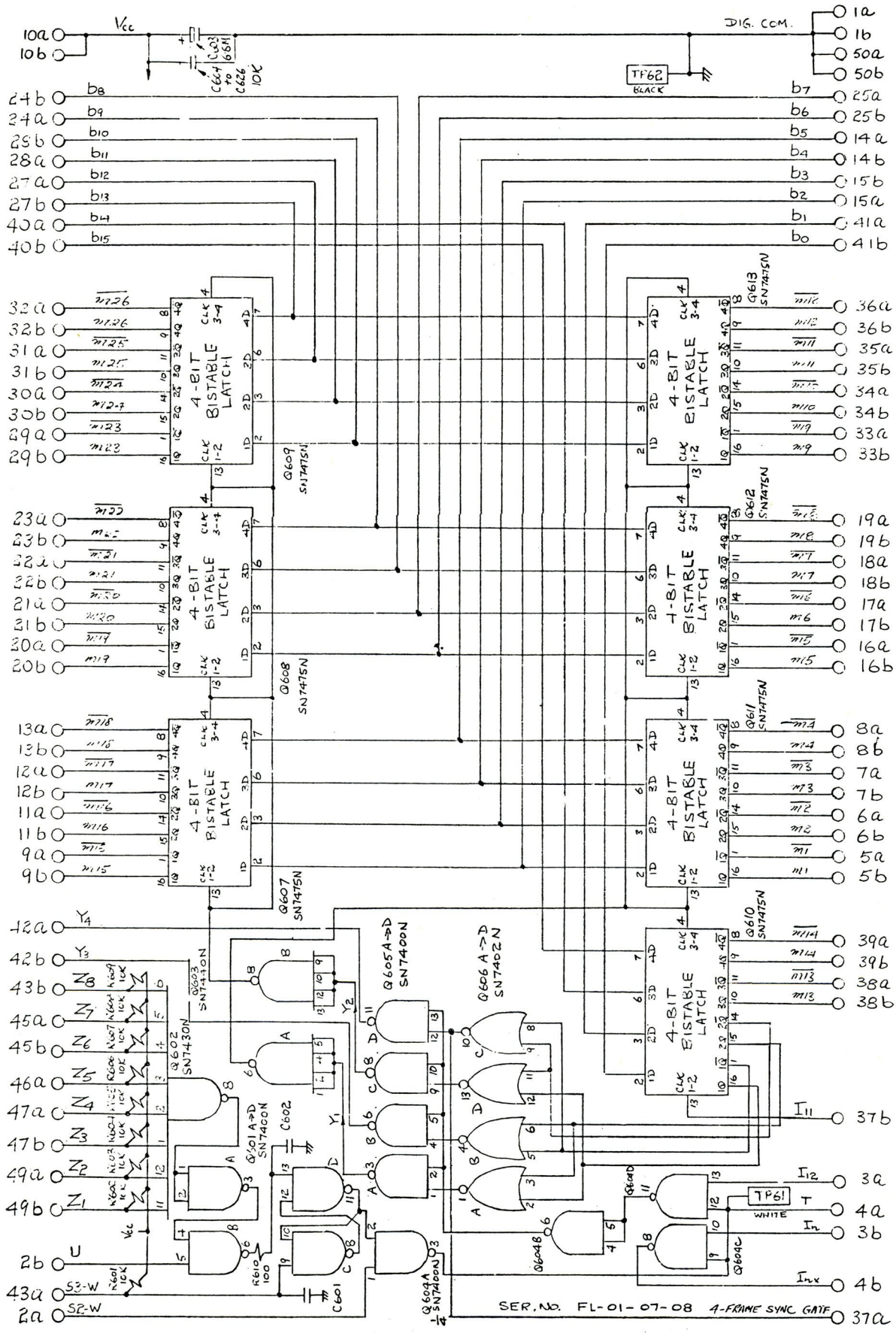


FIG. 22 TIME-OF-DAY STORE AND PRESET-STOP GENERATOR

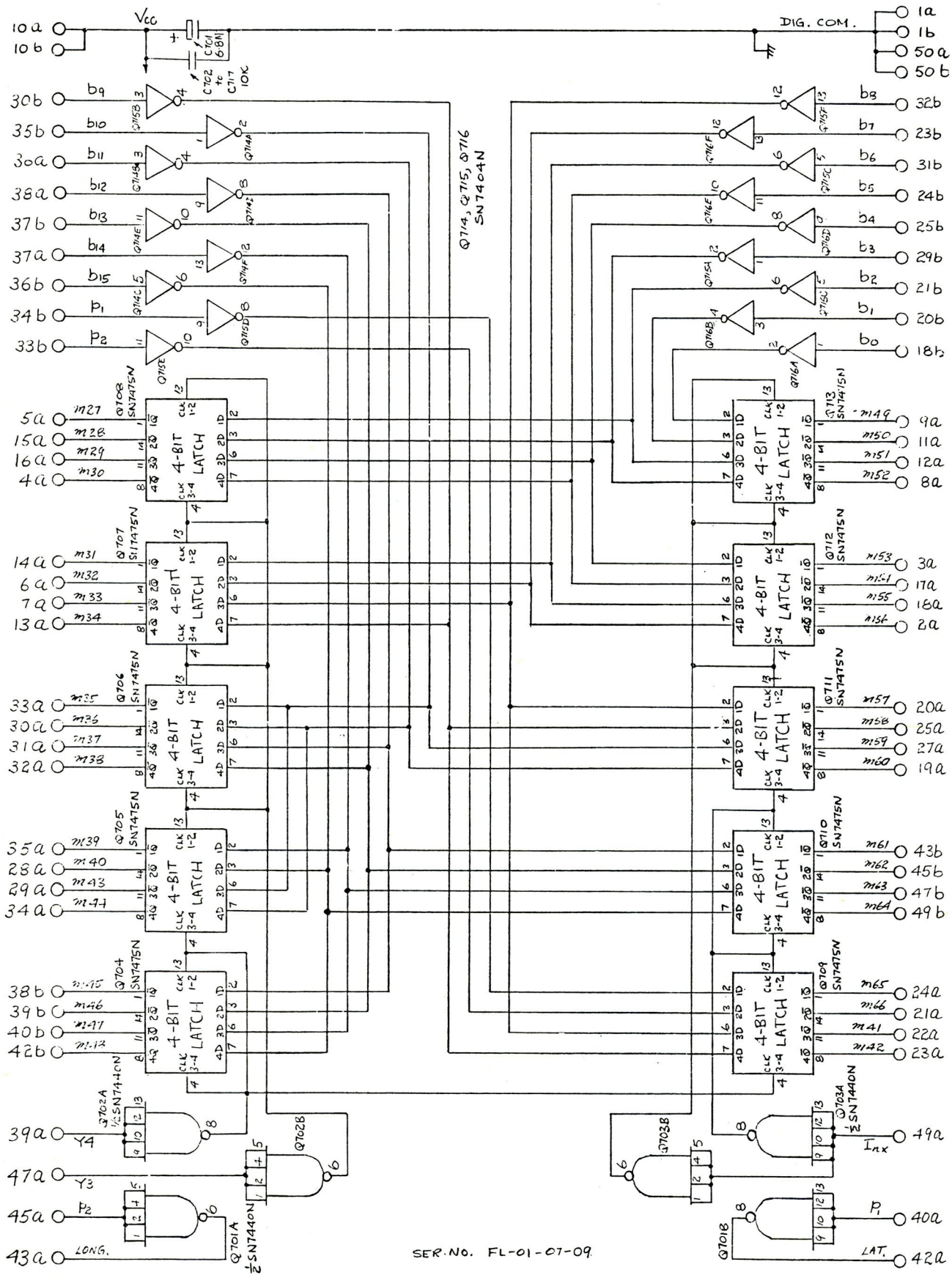


FIG. 23 SELECTED DATA AND FIXED DATA STORE

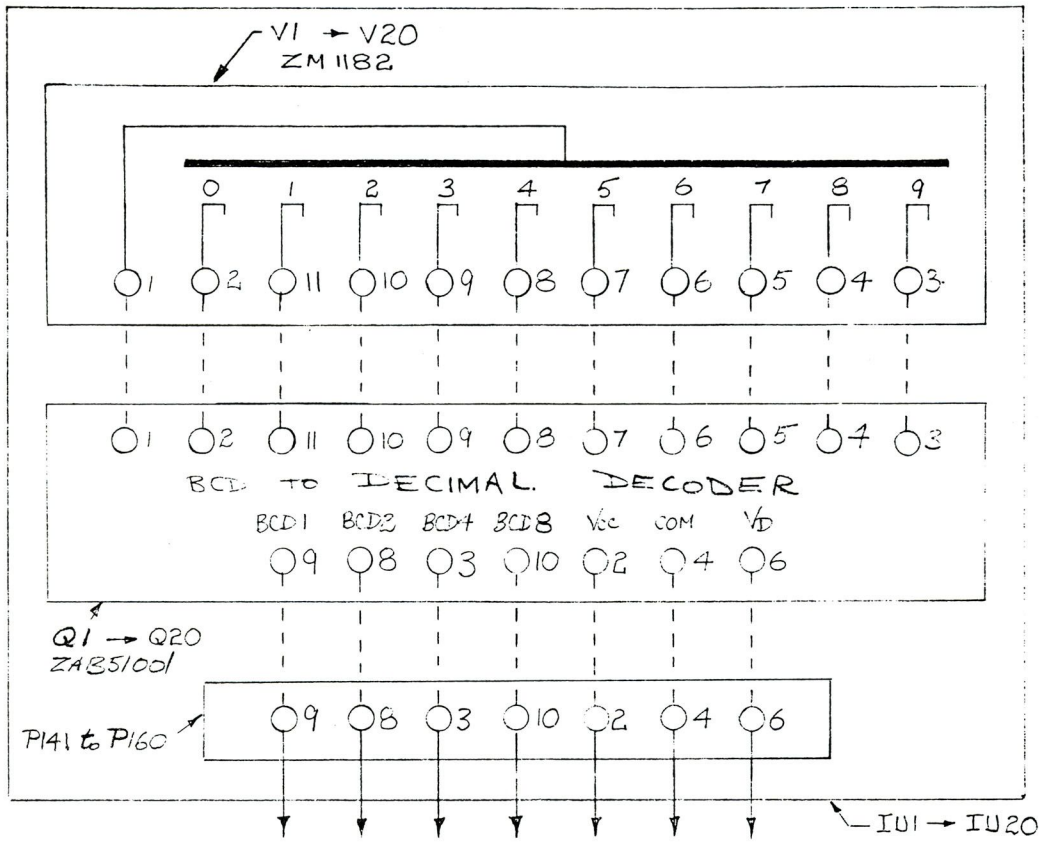


FIG. 24(a) NUMERIC INDICATOR UNIT

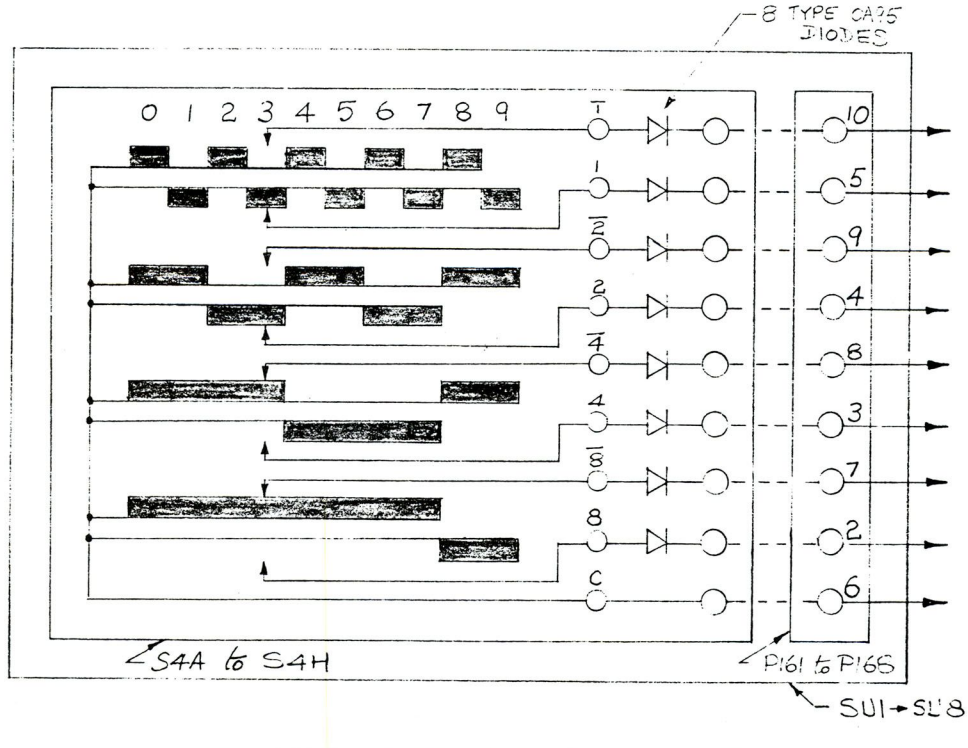


FIG. 24(b) PRESET STOP SWITCH UNIT

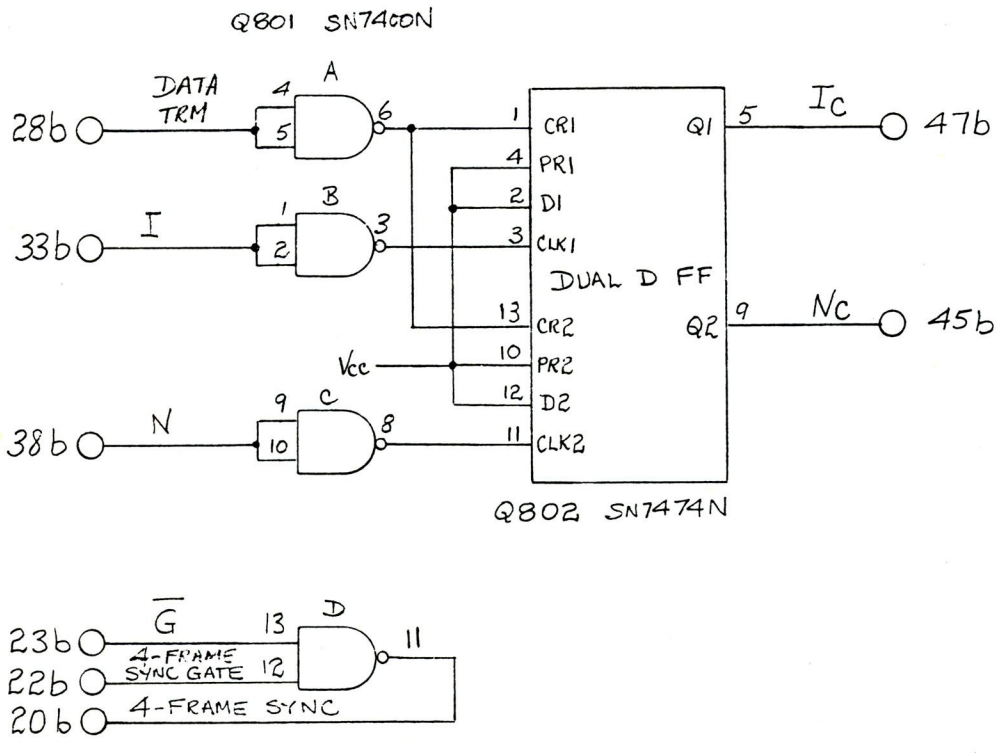


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FIG. 25 COMPUTER INTERRUPT CONTROLLER

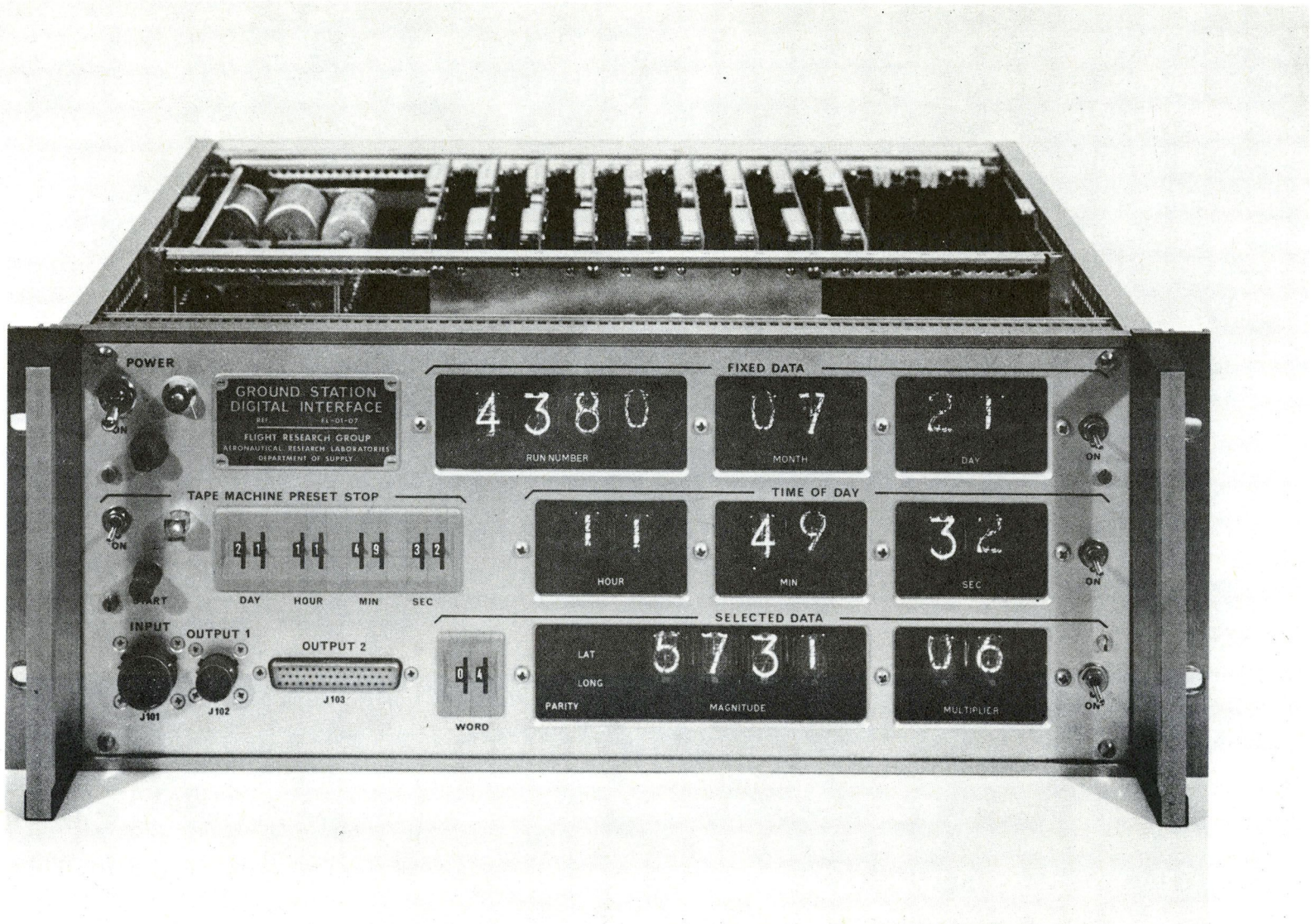

FIG. 26 FRONT VIEW OF GROUND STATION DIGITAL INTERFACE

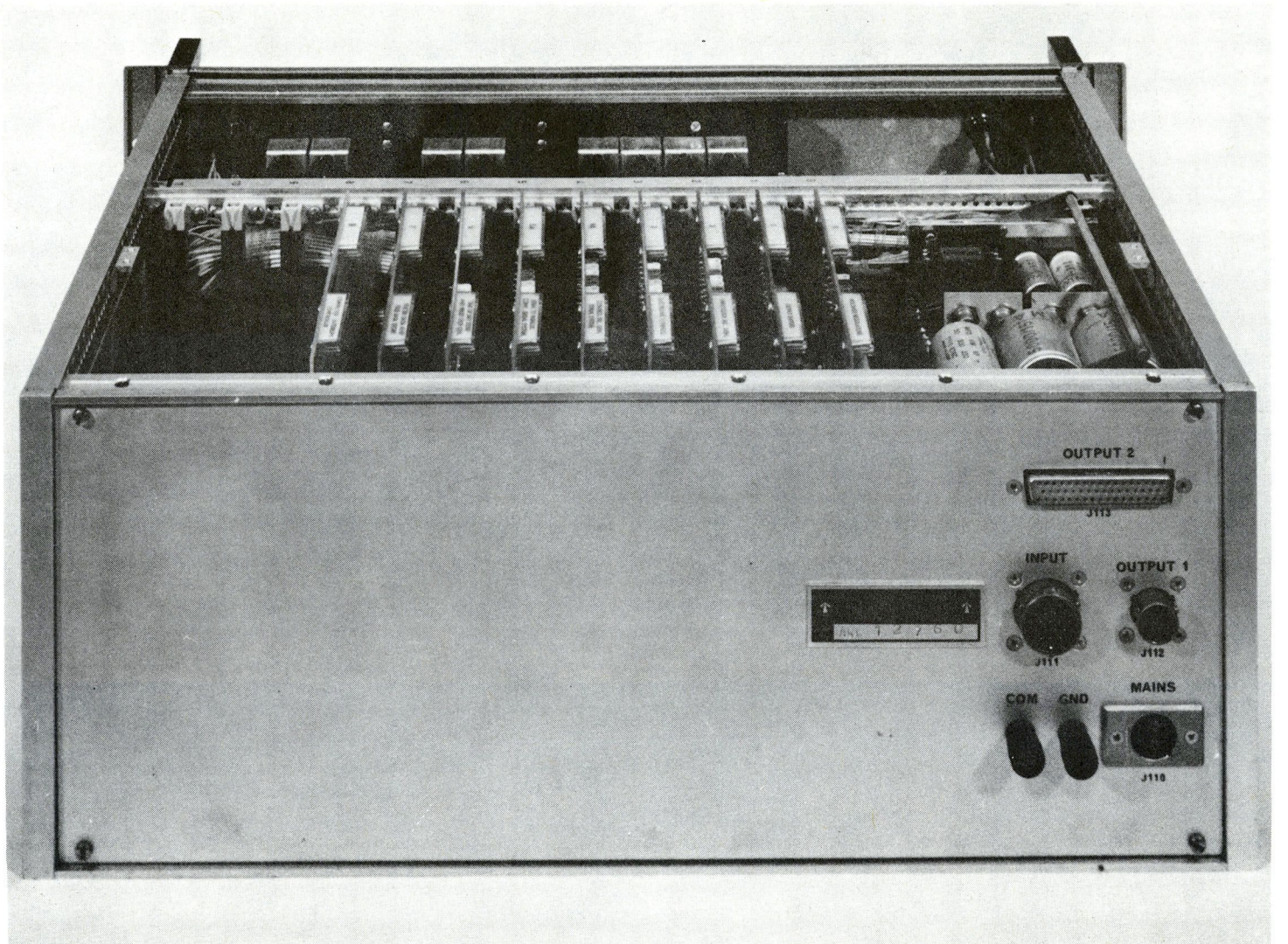

FIG. 27 REAR VIEW OF GROUND STATION DIGITAL INTERFACE

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